Micro-Transfer Printing with x-Chips
X-Celeprint – A Quick Overview

- What do we offer?
  - Licensing of the MTP technology
  - Technical assistance for MTP
  - Prototype building services
  - Production of MTP stamps

- What do our partners offer?
  - MTP production tools
  - MTP ready source material
  - MTP in higher volume

- X-Celeprint develops advanced microelectronic assembly solutions
- Core technology, Micro Transfer Printing, invented by the Professor John Rogers UICU.
- Headquarters - Cork, Ireland
- US development site - Research Triangle Park, NC
The Micro Transfer Printing Process

**Step 1:** Fabricate x-chip devices on source wafer with sacrificial under layer and tether system

**Step 2:** Create custom tailored stamp to transfer devices

**Step 3:** Chemical etch of sacrificial layer on source wafer, creating suspended devices

**Step 4:** Align stamp with devices to be transferred

**Step 5:** Lift stamp and break tethers, removing devices

**Step 6:** Stamp contacts target wafer and transfers devices

Repeat for as many devices/designs as desired...
Attributes of MTP Technology

• Manipulate objects that are too small, numerous, fragile, or otherwise difficult to handle by other means
• Massively parallel high-throughput micro-assembly
• Decouples growth (high temp, lattice constraints) and usage (glass, plastic, ceramic) of high-performance materials
• Tolerant to wafer size mismatch
• Uses device “source” wafer efficiently
• Printing tool scales to large format target substrates, suitable for high volume manufacturing
• Effective for “area multiplication” (geometric magnification)
Why the MTP the solution?

<table>
<thead>
<tr>
<th>Performance</th>
<th>Cost</th>
<th>Time-to-Market</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Reducing parasitic loss by using ultra short interconnects</td>
<td>• Using low-cost, massively parallel transfer</td>
<td>• Combining x-chips produced in different fabs and re-using them in multiple</td>
</tr>
<tr>
<td>• Separately manufacturing component functions using the optimal material</td>
<td>• Fabricating only the needed functions on expensive non silicon</td>
<td>designs allows one to manufacture many different advanced circuit designs.</td>
</tr>
<tr>
<td>and technology node then recombining with x-chip “chip-on-chip” interconnect</td>
<td>semiconductors</td>
<td>Compatible with todays 2.5D and chip-on-chip(3D) advanced packaging solutions.</td>
</tr>
<tr>
<td>• Thin devices easily transferred</td>
<td>• Geometric Magnification of the source material (see later slides)</td>
<td>• Leverage current X-Celeprint partners to prepare print ready source material</td>
</tr>
<tr>
<td>• Highly accurate placement of x-Chips to target substrate, currently 1.5um</td>
<td>• Reducing die size, increasing yield with x-chips chip-on-chip</td>
<td>and print in volume.</td>
</tr>
<tr>
<td>3 sigma with a roadmap to 0.5um 3 sigma.</td>
<td>interconnect solutions (3D)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Low cost Thin Film Interconnect (TFI) for chip to chip interconnection</td>
<td></td>
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</table>
There are 4 main components needed to enable MTP in order to create an interconnected solution:

- Release ready source material
- MTP Stamp
- MTP tool
- Target wafer / substrate
Fabrication of Source Wafers of x-chips

X-Celeprint has partnered with X-Fab to use the XT018 SOI process print ready.
X-Celeprint is working with other partners to develop similar SOI and III-V capabilities.
X-Celeprint offers services in order to create print ready source wafers for prototyping in both North Carolina and Cork Ireland.
X-Celeprint can also perform a technology transfer and training for customers and customer partners.

Fabrication

- Si CMOS on SOI
- InP Optoelectronics
- GaAs Transistors
- GaN RF components
- GaAs Lasers
Methods to Create X-Chips

### SOI x-chips
- Use wafer with base <100> or <111> crystal plane orientation
- Remove silicon under x-chips with TMAH or KOH
  *Oxide under x-chips acts as a barrier against etch of x-chips above*

### III-V x-chips
- If III-V material is grown on silicon <100> or <111> substrate, a TMAH etches silicon underneath x-chips while not etching III-V material

**Table of Release systems**

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Release Layer</th>
<th>Release Agent</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon on Insulator (SOI)</td>
<td>Buried Oxide (BOX) of SOI</td>
<td>HF (conc.)</td>
</tr>
<tr>
<td>GaAs</td>
<td>AlGaAs</td>
<td>HF or HCl</td>
</tr>
<tr>
<td>Si (111)</td>
<td>Si (111)</td>
<td>KOH or TMAH (hot)</td>
</tr>
<tr>
<td>GaAs</td>
<td>InAlP</td>
<td>HCl</td>
</tr>
<tr>
<td>InP</td>
<td>InGa(Al)As</td>
<td>FeCl3 or H3PO4:H2O2 or citric acid: peroxide</td>
</tr>
<tr>
<td>InP (InGaAs)</td>
<td>InP</td>
<td>HCl</td>
</tr>
<tr>
<td>Silicon on Insulator (SOI)</td>
<td>Si (100)</td>
<td>KOH or TMAH (hot)</td>
</tr>
</tbody>
</table>
Device Singulation/Definition

Singulate devices by etching through the device layer(s) and landing on the release layer.

**Dry Chemistry**

1. Coat and Pattern Wafer
2. Descum
3. Dry Etch in RIE to Release Layer
4. Strip Photoresist
5. Descum

* For photoresist tethers, the etch will land on the handle rather than the release layer.
Create Anchor-Tether System

**Process 1**
**Dielectric Tether**

1. Blanket Coat Dielectric
2. Coat and Pattern Photoresist for A-T System
3. Dry Etch
4. Strip Photoresist
5. Descum

**Process 2**
**Photoresist Tether**

1. Coat and Pattern Wafer
2. Coat and Pattern Wafer

Generally, the tether surrounds the device on all sides, and inlets to the release layer are patterned.
**X-FAB MTP process**

Our partner company X-FAB Erfurt has developed a pilot line for MTP

- Industry first pilot line for the integration of smart systems by MTP.
- XFab is currently integrating Customer Specific projects into their pilot line.
- XFab and X-Celeprint are currently working to develop a PDK for the XT018 print ready process.
- X-Celeprint can connect you to XFab.

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**Micro-Transfer-Printing – Application examples**

- ASIC integration enabling System-in-Package solutions
- Heterogeneous integration of GaAs Hall plates for magnetic sensors
- Optical filters for photosensitive sensors

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https://www.xfab.com/technology/wlp-3d-int
1. A stamp master is fabricated in silicon with standard fab photo processes.
2. PDMS is then cast between the stamp master and a sheet of glass in a glass mold.
3. The assembly is then cured, and the glass and PDMS are separated from the stamp master.
**Geometric Magnification**

- MTP allows for devices to be fabricated at any foundry on its’ native substrate and densely packed.
- A custom stamp is created that will match the pitch of the receiving substrate in X and Y dimension.
- The source material with a x-Chip pitch which is an interval of the target substrate.
- In the example above, there are 3 x-Chip intervals in the X and 5 x-Chip intervals in the Y.
- This then allows for 15 separate prints to occur within a single area of the source material.
**First Print sequence**

1. Stamp’s posts adhere to x-chips via van der Waals force
2. Stamp’s visco-elastic behavior
   - Fast separation speed in pick-up regime
   - Slow separation speed in printing regime
3. Lifting stamp breaks tethers and removes x-chips
4. Massively parallel selective pick-up and transfer of thousands of x-chips
5. Readily transfers ultra-thin x-chips

- Stamp contacts destination substrate and x-chips stick to new surface
- Placement with controllable pitch and pattern
- A relative “slow” separation speed is used in the 10s of um range to allow the x-Chip to be printed to the substrate.

Second print sequence

Third, Fourth and Fifth Prints – Note fifth starts new destination wafer
First print of second type of x-Chip on previously printed wafer

• MTP also allows for a second x-Chip to be printed on the same target wafer.
• This second x-Chip can be of the same material type or a different material type.
• The second x-Chip can also perform a different function, i.e. 1\textsuperscript{st} could be a laser, while the second could be a sensor.
MTP Tool

• Currently there are 2 companies producing tools:
  • X Display Corporation
  • ASM/Amicra

• All tools are built in order to maximize the following:
  • Robust, automated toolset for mass-transfer consists of proprietary stamp, motion platform, and optics for precision alignment.
    • MES (manufacturing execution system) interfaceable
    • Demonstrated >15,000 transfer cycles per stamp
  • All elements of the micro-transfer print process are CMOS fab-compatible
  • 200 -300 mm capability
  • Gen 4.5 Panel tools being planned
  • All tools have AOI Cognex software for print QA

Above is a fully automated 200mm tool offered by X Display Ltd.
Nova+ MTP Manufacturing System

Features
- Fully automatic high volume manufacturing system
- ISO 4 clean room class
- Up to 300x300mm source wafer
- Up to 450x450mm destination substrate (wafer or panel)
- 50x50mm (max) stamp array
- ~40 sec cycle time for 1 stamp transfer with 2 point alignment
- ± 1.5µm @ 3σ placement accuracy
- Dual bond head system
- Look-through bond head
- Automatic tip-tilt adjustment

Additional
- ASM AMICRA
- AFC+ for R&D and low volume manufacturing
- NANO: ± 0.5µm @ 3σ placement accuracy
- ~40-65 sec cycle time, 20x20mm (max) stamp array

Contact Johann Weinhändler: Johann.Weinhaendler@asmpt.com
Micro Transfer Printing in Action

Printing an array of 20x28 devices onto a silicon target substrate

Objective field of view shows 1 field.

1. pick-up,
2. print,
3. clean.
[repeat]
MTP Target Substrate

- MTP target substrates can be a variety of materials (Si, glass, plastic, ceramic and surfaces (smooth, rough etc.).
- Target use is dependent on the application.
  - x-chip onto 2.5D interposer (Heterogeneous Integration)
  - x-chip onto silicon device wafer (chip-on-chip) ie. 3D

Demonstrated Target Substrates

- Silicon CMOS
- Glass
- Plastic
- Ceramic
  - Smooth surfaces
  - Rough surfaces
  - Non-planar

Printable devices have been made from many important technologies
  - Gallium Arsenide, Gallium Nitride, Indium Phosphide and Silicon
Ultra-Thin X-Chips Enable Standard Thin Film Interconnect

1. TiW/Cu Seed Layer
2. Seed Layer
3. Resist
4. Plate up
5. Strip resist

Create seed metal and then electrochemically grow Cu on seed metal where desired to interconnect printed devices with wafer.

Integration of GaN HEMTs onto Silicon CMOS by Micro Transfer Printing

High-Brightness Displays Made with Micro-Transfer Printed Flip-Chip microLEDs
MTP – for Bumped Devices & Modules

1) Transfer printing

2) Electroplating of Cu redistribution lines (RDL)

3) Polyimide or epoxy dielectric

Close up view of dielet with Cu RDL

4) Electroplating of NiAu pads

5) Solder bumps by ball drop method

MTP printed devices can be connected and bumped with standard semiconductor processing.
MTP Print Yield – Semprius Solar Cells

• Fabricated surface mountable package with 600 µm, 3J solar cell
• Smaller cell provides competitive advantages in concentrated photovoltaics
• Thousands of target wafers printed in pilot production
• Highly reliable package, >25 billion cell hours in field, passed rigorous reliability testing

Sample of 105 interposer wafers, 4866 die per wafer
• Solar cells printed from 150 mm GaAs wafer to 150 mm ceramic wafer
• Printed with a 24x24 post array stamp, 13 print cycles per target wafer
• Average print yield of 99.3%

Summary Statistics

<table>
<thead>
<tr>
<th>Summary</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean</td>
<td>0.993379</td>
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<tr>
<td>Std Dev</td>
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<tr>
<td>Std Err Mean</td>
<td>0.0004673</td>
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<tr>
<td>Upper 95% Mean</td>
<td>0.9945453</td>
</tr>
<tr>
<td>Lower 95% Mean</td>
<td>0.9926128</td>
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<tr>
<td>N</td>
<td>105</td>
</tr>
</tbody>
</table>

Print Yield Distribution of 105 interposer wafers

24.5 kW CPV system

150 mm ceramic wafer with 4866 printed solar cells
MTP Reliability Data

- Many tests were completed on the Semprius solar modules
- These modules consisted of 3J solar cells printed to rough Alumina ceramic wafers with a 3um print adhesive.
- All testing showed passing reliability results.
- No system degradation was also noted at multiple sites. Below is a review of the Tucson Arizona site after more than 3 years.

<table>
<thead>
<tr>
<th>IEC 62108 Testing (as of Jan 2013)</th>
</tr>
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<tbody>
<tr>
<td>Section</td>
</tr>
<tr>
<td>10.3</td>
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<tr>
<td>10.15</td>
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<tr>
<td>10.16</td>
</tr>
</tbody>
</table>

No System Degradation After > 3 Years at Tucson

- 1 kW system installed in November 2011
- Plots taken after cleaning, but ignores effects of temperature and spectrum

No measureable degradation after 40 months on sun

All IEC testing of CPV modules passed
MTP Print Yield – Display Print Drivers on Glass

Printed µICs

270x70 µm ICs

Display Print Yield

Summary Statistics

<table>
<thead>
<tr>
<th>statistic</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean</td>
<td>0.9995867</td>
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<tr>
<td>Std Dev</td>
<td>0.0001685</td>
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<tr>
<td>Std Err Mean</td>
<td>0.0000435</td>
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<tr>
<td>Upper 95% Mean</td>
<td>0.99968</td>
</tr>
<tr>
<td>Lower 95% Mean</td>
<td>0.9994934</td>
</tr>
<tr>
<td>N</td>
<td>15</td>
</tr>
</tbody>
</table>

Print yield of 15 displays, each with 46,080 µICs

- 15 displays were made (>690k transferred devices)
- Mean print yield: 99.96%
- Displacement at 3σ: +/- 1.5um

Placement Accuracy, Micro-drivers for Emissive Display

Displacement distribution of 1 display
MTP Print Repair

Repair of the printing can be achieved post printing of the target substrate in multiple ways using a single post stamp to pick and print single chips depending on the final yield need.

- Printing to a non-printed site with no defects is possible
  - Defect on source does not allow x-Chip to print.
  - Defect on the bottom of the x-Chip that does not allow to print

- A second site to print if the primary site is defective
  - A defect on the target site that does not allow printing to occur
  - A defective x-Chip has been printed

- Redundant printing of devices to allow for “defective” chips
  - An application that needs 100% yield
MTP Applications

- HEMTs
- MEMS
- Laser Diodes
- μLEDs
- ICs
- RF Sensors
- Interconnects
- Solar PVCs
- Memory
Printed Multi-junction Solar Cell

- Smaller cell provides competitive advantages in concentrated photovoltaics
- 600 µm, 3 junction solar cell uses µTP to fabricate surface mountable package
- Thousands of target wafers printed to date
- Highly reliable package, >25 billion cell hours in field, passed rigorous chamber testing
RF GaN HEMTs onto Silicon CMOS

- 5G /RF Single Pole Single Throw (SPST) switch of GaN on SOI
- <0.4 dB insertion loss up to 30 GHz
- 59% reduction in vertical capacitive coupling
- Performance attributed to ability of placing GaN on SOI

**RF Small and large signal characterization of a 3D integrated GaN/RF-SOI SPST switch**

**RF SPST Switch Based on Innovative Heterogeneous GaN/SOI Integration Technique**
GaN Power Electronics Integrated on CMOS

GaN HEMTs Integrated onto CMOS

GaN-on-Si Release Process

![Diagram showing GaN-on-Si Release Process](image)

Source

- **Integration of GaN HEMTs onto Silicon CMOS by Micro Transfer Printing**
- **Printing GaN HEMTs onto Silicon CMOS**

GaN HEMT printed and interconnected on Si CMOS
Photonic Integrated Circuit (PIC)

Benefits:

- **Efficient assembly of multiple heterogeneous materials**
  Lasers, modulators, detectors, driver ICs (analog and logic)

- **Precision alignment at each step**
  Efficient coupling of devices to waveguide wafers

- **Mass-Transfer**
  Scales to high device count as data demands continue to rise

- **Minimized device sizes**
  Significant savings of expensive III-V materials
Photonics Lasers

Transfer-Printed InP Lasers

Pre-processed etched facet lasers

Transfer printed to Si

CW lasing of 1550nm laser on Si

Source
Power 3D IC

Benefits:  • Disaggregation and tight reintegration of many gate drivers and power transistors
  - Minimizes parasitics
    * Increases switching frequency, density, transient response and efficiency
  - Enables high-performance multi-stage hybrid topologies

• Cost reduction
  * Produces 3D ICs which resemble conventional 2D ICs (using conventional packaging)

Option #1
- Gate driver x-chips
  * Loosely-packed SOI
- Power transistor x-chips
  * Tightly-packed SOI, GaAs, GaN
- Monolithic die
  * GaN, GaAs or silicon power transistors
    * Tightly-packed

Option #2
- Power transistor x-chips
  * Tightly-packed SOI, GaAs, GaN
- Monolithic die
  * CMOS IC
    * Gate drivers, control, protection & monitoring
Secure IC

Benefits:

• Integrate x-chips in trusted US advanced packaging facilities
  *Using source wafers produced in US and overseas foundries*

• Provides hardware-based quantifiable assurance
  *For cutting edge ICs produced in untrusted fabs*

• MTP allows for *disaggregated* arrays of security x-chips
  *Further obfuscate functionality*
X-Celeprint’s Work-in-Progress

**X-Chip**
- Large x-Chips over 1mm x 1mm up to 4.5mm x 2.5mm
  - Currently releasing up to 1mm x 1mm square x-Chips and 1.5mm x 100um x-Chips

- Thick chiplets between 50um - 150um thick
  - Currently picking up only released chips proven up to 20um

- Transfer Print from bulk material
  - Standard silicon wafers with no oxide layer
  - III-V material from native substrates
  - Currently using a release layer to undercut chiplets

- Through x-Chip interconnect
  - To allow for additional connectivity through the x-Chip

**Alignment**
- Roadmap to move alignment accuracy to 0.5um 3 sigma
  - Currently printing to 1.5um 3 sigma
Summary: Micro-transfer Printing of x-Chips

- **Small devices**
  - At least as small as 3 µm x 3 µm x 200 nm, and likely much smaller
  - As large as 1 mm x 1 mm, and likely larger

- **High throughput**
  - Up to 65,000 devices printed simultaneously in 1 cycle
  - 30 s per cycle
  - ~7M devices printed per hour

- **High yield**
  - >99.9% per print cycle
  - Precision repair → **effective 100% yield**

- **High accuracy**
  - Demonstrated 1.5 µm @ 3σ
  - Working towards 500 nm

- **Small pitch**
  - Down to 2 µm

- **Substrate flexibility**
  - Materials-agnostic
  - Demonstrated print on Si, glass, ceramic, plastic, smooth, & rough surfaces

- **Heterogeneously integrate** different components on one substrate
  - Materials-agnostic
  - E.g., sensors, LEDs, lasers, interconnects, MEMS, etc.

- **Deterministically disperse devices** produced at high density on target surface

- **Vertically stack** chip-on-chip - 3D
  - For 3D HI devices
  - For multi-junction solar cells

- **Simple** thin film interconnect

- End product is highly **customizable and modular**

- **Cost-effective**
  - Efficient use of material
  - High throughput
Key References by X-Celeprint and select partners

- Interposing of Microelectronics by Micro Transfer Printing to Create 3-D Structures
- Transfer-printing for heterogeneous integration
- Manufacturing Capability of Micro-Transfer Printing
- Scalability and Yield in Elastomer Stamp Micro-Transfer-Printing
- Fan-Out Packaging of Microdevices Assembled Using Micro-Transfer Printing
- Transfer printing by kinetic control of adhesion to an elastomeric stamp
- Kinetically controlled, adhesiveless transfer printing using microstructured stamps
- Process capability and elastomer stamp lifetime in micro transfer printing
- Transferred III-V materials-novel devices and integration