Integrated Power Electronics Components for Integrated Voltage Regulators

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On behalf of the Heterogeneous Integration Roadmap's Integrated Power Electronics Technical Working Group

I. Introduction

Approximately a trillion transistors could be integrated in a System-in-Package (SiP) (Figure 1) by 2030[1] by heterogeneously integrating many CPU, FPGA, AI accelerator, networking, memory, I/O and other chiplets. Chiplet power densities are forecast to increase to 2W/mm^2 average with >9W/mm^2 hotspots.[2] SiP performance is limited by the ability to deliver power to and remove heat from the SiP.

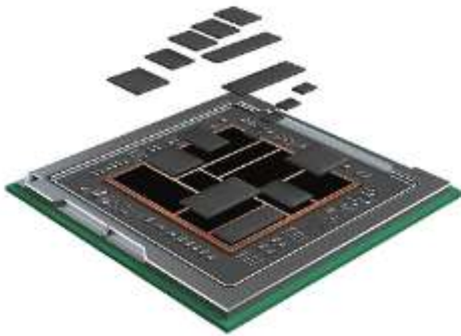

Figure 1: System-in-Package[3]

Fine-grain power management offers the opportunity significantly to improve energy efficiency (performance per watt) by supplying the minimal voltage required at any given time to each load but requires many Integrated Voltage Regulators (IVRs) with fast transient response embedded in the SiP in close proximity to the load die (Figure 2).[4,5,6,7,8,9,10,11]

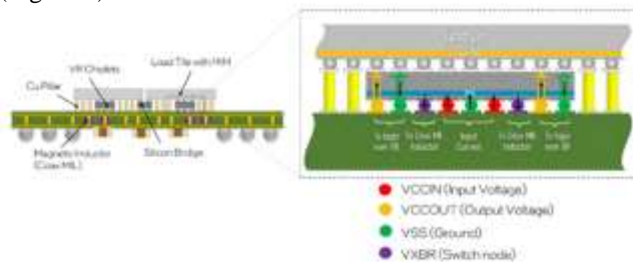

Figure 2: Integrated Power Electronics Component[4]

Load power dissipation is highly dependent on voltage, increasing more than quadratically with supply voltage considering thermal degradation and leakage power in addition to dynamic power. For <10nm processes, power increases by 3% for every 10mV increase in supply voltage.[12] Hence, precise voltage regulation is required because the alternative of using large voltage margins reduce the performance and power efficiency. IVRs are required to minimize the power distribution network (PDN) impedance and supply loads with voltages within a tightly controlled operating range. This need is escalating with advanced CMOS nodes whose operating voltage is in close proximity to threshold voltage. External board-mounted voltage regulators cannot supply accurate voltages for fine-grain power management due to their high PDN impedance, so the way forward is board-mounted DC-DC converters that step down the system bus voltage to an intermediate voltage which is then input to IVRs that perform voltage regulation and bypasses the majority of the PDN impedance.[13,14,15]

Meeting IVR's extremely challenging requirements necessitates using the optimal manufacturing technology to produce each of its constituent components – power transistors, gate drivers, controllers, inductors and capacitors – and heterogeneously integrating them in an Integrated Power Electronics Component (IPEC) for subsequent integration of IVRs in SiPs. This article summarizes the IPEC roadmap described in detail in the Heterogeneous Integration Roadmap.[16]

II. Requirements

IPEC requirements include the following:

- >5V input voltage[4] to balance being low enough to support high switching frequency and high enough to reduce the PDN's routing loss for support escalating output power (Figure 3) and reduce the number of power/ground pins, which compete with I/O.

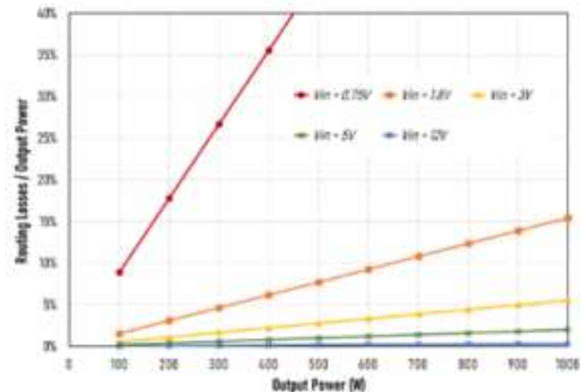

Figure 3: Routing Losses[4]

- 0.6V to 1.2V output voltage[4] to support SiPs integrating a diversity of load die made using different process nodes and having different voltage requirements. Lower voltages minimize power consumption during power-saving operating modes and higher voltages maximize performance during peak operating modes.
- 10-20A/mm^2 output current density[4] to keep up with scaling to advanced CMOS nodes escalating current density. High-end SiPs will draw more than 1,000A in the near future,

- >90% efficiency[4] to reduce heat dissipation which is a major challenge, since IVRs share the SiP's limited thermal envelope with the load die, and IVRs are located in close proximity Power loss is due to conduction loss, switching loss and charge loss. At IVR's target current density and switching frequency, minimizing conduction loss in the interconnects and minimizing the inductive and capacitive parasitics between the power transistors, gate drivers and power transistors is essential.[17]
- 10-25MHz switching frequency[4] to balance being low enough to support low duty cycles (output voltage divided by input voltage) and high efficiency and high enough to reduce the size of the inductors and capacitors and to increase the control loop bandwidth, improving transient response. Low bandwidth VRs require additional decoupling capacitors to make up for their slow response time. Small, modular building blocks that may be used in a wide range of SiPs for high performance computing, mobile, automotive, medical, and aerospace and defense applications having many different load and power delivery requirements.
- Minimal z-height to facilitate integration in close proximity to the load die in a wide range of package architectures.
- Ultra-low thermal resistance to facilitate heat removal.
- High reliability to ensure operation at all times in the safe operating area, which is typically well below the rated voltage, maximum allowable junction temperature and maximum allowable current density, and meet reliability standards.
- Cost-effective to enable IPECs to be used in a wide range of SiPs for many different applications.

Backside power delivery[18,19] improves voltage droop characteristics and enables denser load die signal routing but still requires IVRs for fine-grain power management.

III. Potential Solutions

Potential solutions include a three step approach. First, employ the optimal manufacturing technology to produce each of the IVR's constituent components – power transistors, gate drivers, controllers, inductors and capacitors. Second, heterogeneously integrate these components in an IPEC that may be tested and binned resulting in a known good "die" (KGD) which are not monolithic but rather heterogeneous and employ 3-dimensions. (The controller some capacitors may be integrated in the load die and some capacitors and inductors integrated in the SiP). Third, integrate multiple IPECs in the SiP using a variety of packaging architectures.

Integrated capacitor technologies include electrolytic capacitors, ceramic capacitors and silicon capacitors and are discussed in Part 2 of Chapter 1 of the Heterogeneous Integration Roadmap. Integrated inductor technologies include:

- Small footprint (0201 – 0.2mm x 0.1mm) discrete inductors, using high frequency (100MHz+) polymer-loaded composites or fired magnetic material, with low profile (less than 0.1 to 0.3 mm). These components can be used in a PSiP platform, either as surface mount devices [MuRata], or with copper terminations, embedded in the SOC organic substrate or package [Taiyo Yuden].
- High frequency ferrite cores embedded in 2.5D/3D heterogeneous integration structure using BEOL interconnect processing to provide windings [IMEC].
- Vertical coaxial magnetic composite core inductors[20] integrated in the package substrate by plated through holes drilled in the package substrate and encapsulated with a composite magnetic material [Intel].
- Embedded magnetic on silicon inductors embedded in PCB substrate or package [Wurth].
- Embedded thin film CoZrTa (CZT) combined with copper windings in PCB substrate or package [Tyndall]
- Electroplated planar copper windings with electro-deposited magnetic core [Enachip].
- Vertical inductors based on thin film CZT deposited on the sidewalls of low profile electroplated copper pillars [Tyndall].

Technologies to tightly integrate power transistors, gate drivers and bypass capacitors include:

- Monolithic integration with the load die, such as a Intel's Fully Integrated Voltage Regulators (FIVRs).[21,22] The limitation with this approach is load die made using advanced CMOS technologies have low voltage transistors and very thin metal interconnects so cannot support the target IVR input voltage and current density requirements.
- Monolithic integration to produce an IPEC.[23,24,25] The limitation with this approach is lower performance and higher cost since the optimal manufacturing process for each of these components is different.
- Heterogeneous integration with the load die.[26] The limitation with this approach is increasing the complexity, cost and development time of each load die and high routing loss resulting from the load die's thin metal interconnects.
- Heterogeneous integration in an IPEC for subsequent integration in a SiP.[27]

An example of a heterogeneously integrated IPEC (Figure 4) may be constructed as follows: gallium nitride (GaN), gallium arsenide (GaAs) or silicon power transistors are disaggregated into large arrays of ultra-thin (<15μm), small transferred chips (x-chips) which densely pack the source/drain fingers to minimize their on-resistance • area figure-of-merit, connect gates to both side of the power transistor and minimize lateral current flow in the thin

metal layers made using semiconductor wafer fab. The last step in the wafer fab process is passivation openings to top metal, and the passivation openings are arranged for subsequent RDL interconnects using coarse (>10µm/10µm) line/space (L/S) design rules to the source, drain and gate. Power transistor x-chips are transferred to the bottom side of thin, large area glass substrates with through-substrate vias with their active side facing down towards the package substrate. Similarly, CMOS gate driver x-chips are manufactured on separate silicon wafers and transferred to the top side of the glass substrate with their active side facing up towards the load die. The interconnection distance between the power transistors and gate drivers is just slightly more than 100µm which significantly reduces the parasitics and switching loss.

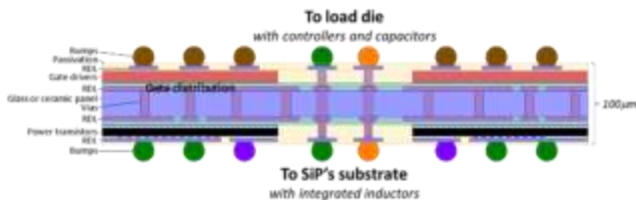

Figure 4: Heterogeneous Integrated IPEC Example[28]

Since the gate driver and power transistor x-chips are ultra-thin and small, panel-level processing (PLP) may be multiple thick redistribution layer (RDL) interconnects that supplement the semiconductor die's thin interconnects to reduce electrical and thermal resistance and support high current density. Lateral current flow in the thin semiconductor die's interconnects are minimized and thick PLP RDL is used for all high current interconnects as well as gate distribution and routing of the control, protection and monitoring signals.

Cost is reduced by: (i) heterogeneously integrating large arrays of small (hence, high yield) x-chips; iii) use of inexpensive PLP with coarse (>10µm / 10µm) L/S design rules versus much smaller wafer-level processing with ultra-fine L/S capabilities for the heterogeneous integration (the majority of the interconnects consume inexpensive glass substrate area rather than expensive semiconductor area), and (iii) producing known good IPECs for testing and binning prior to integration in the SiP.

An example of a potential method for manufacturing IPECs is to use micro transfer printing (MTP)**,** a massively parallel pick-and-place process that efficiently transfers large arrays of ultra-thin (<15µm), small, separately manufactured components from one or more source wafers to destination silicon wafers or large-area glass or ceramic substrates.[29,30,31,32] A fully automatic ISO 4 clean room class system transfers up to 50x50mm arrays of x-chips from source wafers (up to 300mm) to destination wafers (up to 300mm) or panels (up to 450x40mm).[33] By customizing the post spacing of the MTP system's stamp, x-chips tightly packed on the source wafer (maximizing source wafer utilization) are efficiently spread out on the destination substrate. Placement accuracy is +/-1.5µm (3 sigma), which resolves the critical position accuracy requirement for the RDL interconnect process. Die shift issues are eliminated since x-chips are held in place with a thin adhesive layer underneath with RDL on top and no epoxy mold compounds are used.

IV. R&D Opportunities

IPEC R&D opportunities include the following:

- Optimization of separately manufactured components, including power transistors, controllers and gate drivers and thin-film inductors and capacitors for >10MHz switching frequency with >5V input voltage.
- Heterogeneous integration of large arrays of ultra-thin separately manufactured components using state-of-the-art PLP technologies on large area substrates with through substrate vias and multiple thick RDL interconnects.
- Use of advanced topologies, such as multi-level buck converters and hybrid switched capacitor / switched inductor converters which reduce voltage requirements and improve performance but require many power transistors, gate drivers and passive components, enabled by heterogeneous integration of arrays of separately-manufactured components.[34,35,36]
- Design technology co-optimization[37] and electronic Design Automation (EDA) tools for the holistic co-design optimization, simulation and integration of separately manufactured IVR components. A variety of stack-ups, layer maps and models, including measured versus modeled correlation and improving load energy efficiency through improving the PDN and fine-grain power management is required.

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References

[1] A. Kelleher, Moore s Law - Now and in the Future, February 16, 2022, Intel Newsroom.

[2] M. Iyengar, Thermal Technical Working Group, Working Group Meeting 1: 2021 IEEE Heterogeneous Integration Roadmap, February 2021.

[3] J. Park, Chiplets and Heterogeneous Packaging Are Changing System Design and Analysis.

[4] K. Radhakrishnan, Challenges and Innovations in Microprocessor Power Delivery, IEEE Electronics Packaging Society Silicon Valley Area Chapter webinar, June 22, 2002.

[5] K. Radhakrishnan et al, Power Delivery for High Performance Microprocessors – Challenges, Solutions and Future Trends, IEEE Transactions on Components, Packaging and Manufacturing Technology, Volume 11, Issue 4, April 2021.

[6] V. De et al, Fine-grain power management in manycore processor and System-on-Chip (SoC) designs, IEEE/ACM International Conference on Computer-Aided Design, 2015.

[7] V. De, System-Level Power Management Strategies for Integrated Platforms, PwrSoC, 5 November 2020.

[8] P. Zou et al, Powering 5G Era Computing Platforms – the Road toward Integrated Power Delivery, 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), May 2019.

[9] X. Zhen et al, Power Management for Multicore Processors via Heterogeneous Voltage Regulation and Machine Learning Enabled Adaptation, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume: 27, Issue: 11, Nov. 2019

[10] D. Kantor, Power Delivery in a Modern Processor, Real World Technologies, 2020.

[11] S. Kulkarni, Voltage Regulators with Integrated Inductors on Chip vs in Package, Applied Power Electronics Conference and Exposition, 2020.

[12] F. Carobolante, PwrSoC at an Inflection Point: From R&D to Market Relevance, Applied Power Electronics Conference and Exposition, 2021.

[13] J. Douglas, Microprocessor Power Delivery Challenges, Applied Power Electronics Conference and Exposition, 2020.

[14] H. Tamdem, 48V Sever Platform Power Architecture and Design Challenges, IEEE Applied Power Electronics Conference and Exposition, 2020.

[15] S. Chakraborty, 54V Power Delivery Architecture for VRMS, IEEE Applied Power Electronics Conference and Exposition, 2020.

[16] Integrated Power Electronics Chapter 10, Heterogeneous Integration Roadmap, 2021 edition, IEEE Electronics Packaging Society.

[17] T. Hegarty, Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics, Texas Instruments' Analog Applications Journal, AAJ Q3 2016.

[18] D. Patel, Imec Demonstrates Backside Power Delivery Network for Enhanced System Performance, EE Power, June 29, 2021.

[19] P. Alcorn, Intel Process Roadmap Through 2025: Renamed Process Nodes, Angstrom Era Begins, Tom's Hardware, July 26, 2021.

[20] K. Bharath et al, Integrated Voltage Regulator Efficiency Improvement using Coaxial Magnetic Composite Core Inductors, Electronic Components and Technology Conference, 2021.

[21] E. Burton, FIVR – Fully Integrated Voltage Regulators on 4th Generation Intel® Core™ SoCs, IEEE Applied Power Electronics Conference and Exposition, 2014.

[22] M. Sankarasubramanian et al, Magnetic Inductor Arrays for Intel® Fully Integrated Voltage Regulator (FIVR) on 10th generation Intel® Core™ SoCs, IEEE 70th Electronic Components and Technology Conference (ECTC), 2020.

[23] J. Doyle et al, A Low Cost 100 MHz 2-Stage PSiP and Evolution to a Co-Packaged/Fully-Integrated Voltage Regulator for SoC Power Delivery, 2019 IEEE Custom Integrated Circuits Conference (CICC).

[24] P. Zou, A 100MHz IVR PMIC with On-silicon Magnetic Thin Film Inductors, PwrSoC 2018.

[25] X. Liu et al, A 50MHz 5V 3W 90% Efficiency 3-Level Buck Converter with Real-Time Calibration and Wide Output Range for Fast-DVS in 65nm CMOS, 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits).

[26] N. Sturcken, Efficient On-chip Power Conversion, Power SoC 2020.

[27] P. Vivet et al, A 220GOPS 96 Core Processor with 6 Chiplets 3D Stacked on an Active Interposer offers 0.6ns/mm Latency, 3Tb/s/mm^2 Inter-Chiplet Interconnects and 156mW/mm^2@ 82%-Peak-Efficiency DC-DC Converters, 2020 IEEE International Solid- State Circuits Conference, 2020.

[28] B. Conner, Integrated Power Electronics Components for Integrated Voltage Regulators and Power Modules, 2021 Power Supply on Chip Workshop, October 27, 2021.

[29] C. Bower et al, Micro-Transfer-Printing: Heterogeneous integration of microscale semiconductor devices using elastomer stamps, IEEE SENSORS, 2014.

[30] K. Osalt et al, Interposing of Microelectronics by Micro Transfer Printing to Create 3-D Structures, Electronic Components and Technology Conference, June 2020.

[31] B. Conner et al, Panel-Level Heterogeneous Integration Technology for Analog ICs, August/September 2021 Semiconductor Digest.

[32] R. Lerner et al, Commercial Sweet Spots for GaN and CMOS Integration by Micro-Transfer-Printing, 15th International Seminar On Power Semiconductors, January 2021.

[33] ASM AMICRA Unveils Industry's First Manufacturing Systems Incorporating X-Celeprint's MTP Technology for High Volume Heterogeneous Integration Of Ultra-thin Chips, April 2021.

[34] R. Pilawa-Podgurski, Hybrid and Resonant Switched-Capacitor Converters: Achieving Ultra Efficient and Compact High Step-down DC-DC Power Conversion for Datacenter Application, Applied Power Electronics Conference and Exposition, 2021.

[35] S. Safwat, A Fully Integrated Li-Ion-Compatible Hybrid Four-Level DC–DC Converter in 28-nm FDSOI, IEEE Journal of Solid-State Circuits, Volume: 54, Issue: 3, March 2019.

[36] G. Villar Piqué et al, 3-Level Buck Converter Analysis and Specific Components Models, CMOS Integrated Switching Power Converters,Springer Science+Business Media, LLC 2011

[37] R. Aitken et al, Predicting future complementary metal–oxide–semiconductor technology – challenges and approaches, IET Computers and Digital Techniques, Volume 10, Issue 6, November 2016, pp. 315-322.