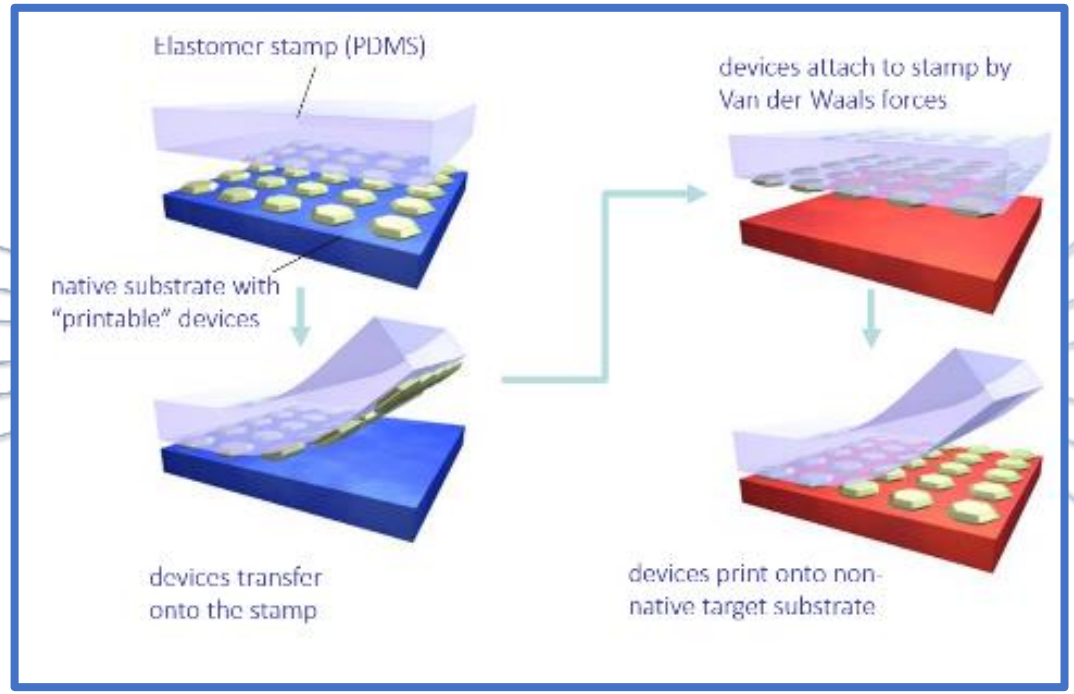
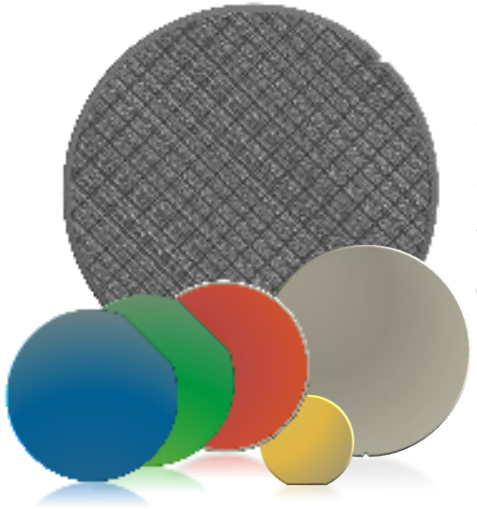
Micro-Transfer Printing with x-Chips

X-Celeprint

Micro Assembly Unlocks New Opportunities for Wafer Fabricated Devices

Elastomer Stamp “Micro-Transfer Printing” (µTP)





Wafer Fabricated Devices
Single-crystal
Fine lithography
(ICs, LEDs, Lasers, etc…)

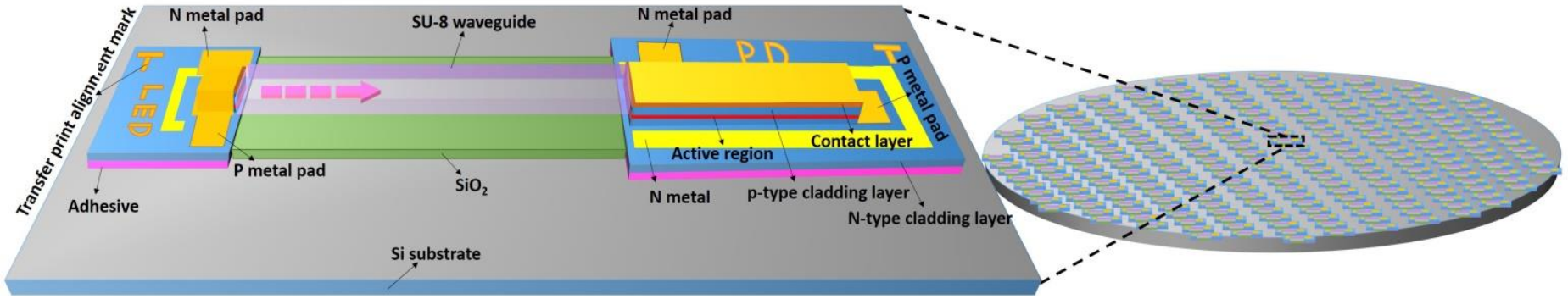
The promise of high-performance devices anywhere

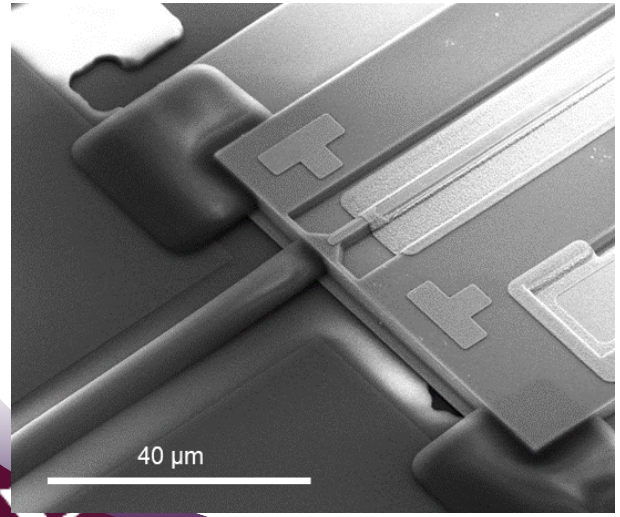
Plastic, Glass, Ceramic, Paper
Other semiconductors

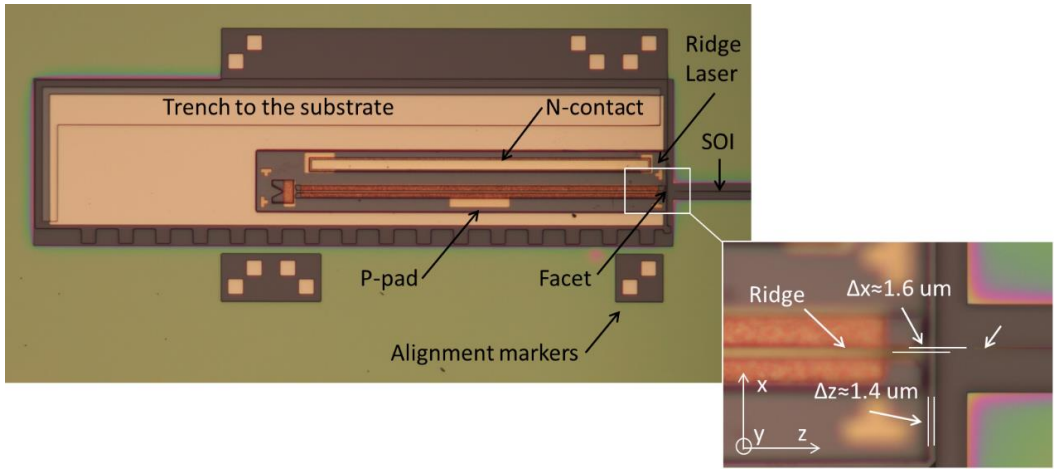
Next generation photonics

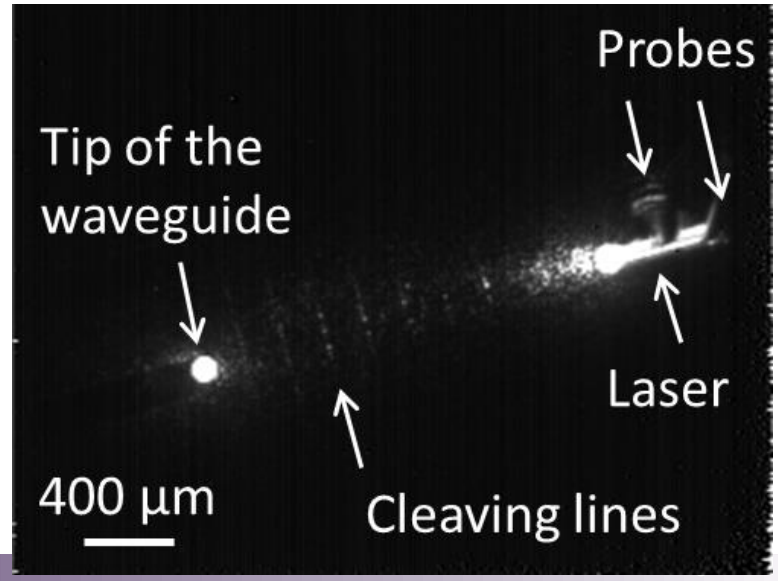
Edge coupling to a polymer and to an SOI waveguide

Complete system on a chip with an LED or a laser



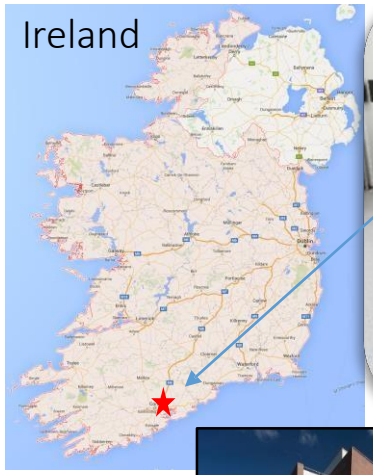


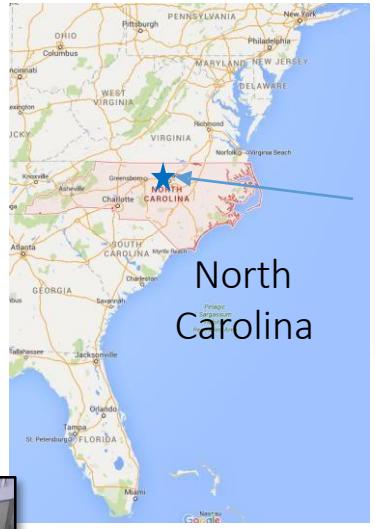


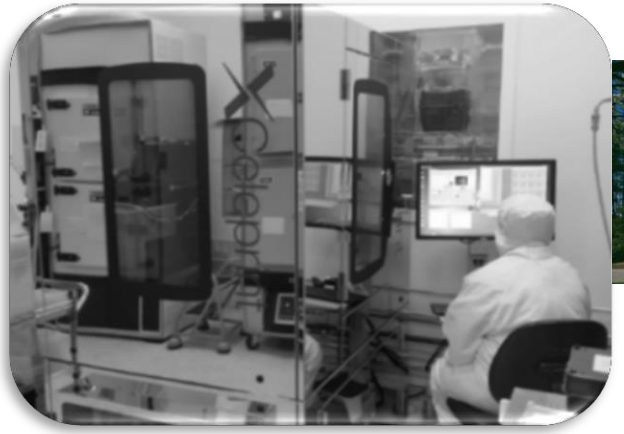


Technology Introduction

X-Celeprint – A Quick Overview







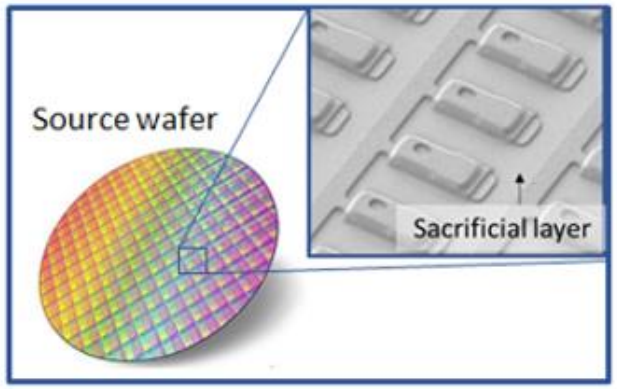
- X-Celeprint develops advanced microelectronic assembly solutions
- Our core technology, Micro Transfer Printing (MTP), invented by Professor John Rogers at the University of Illinois.
- Headquarters are located in Cork, Ireland
- US development site at Research Triangle Park, NC

- **What do we offer?**
  - MTP technology licensing
  - MTP technical support
  - Prototype construction services
  - MTP stamp production

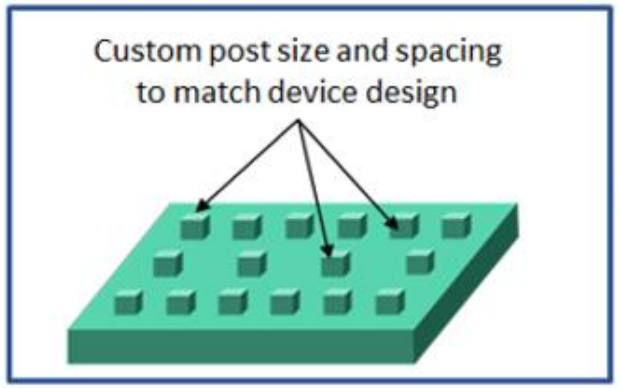
- **What do our partners offer?**
  - MTP production tools
  - MTP-ready source material
  - Higher-volume MTP

The Micro Transfer Printing Process

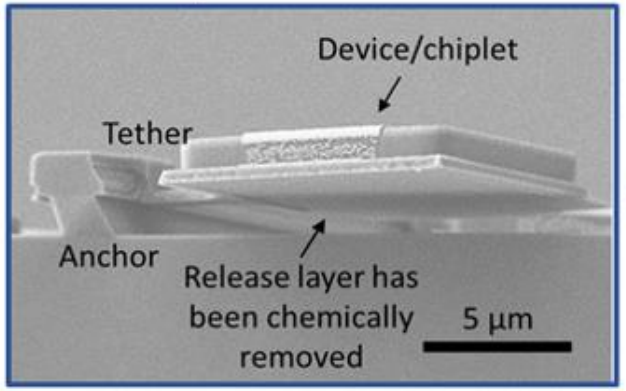
Step 1: Fabricate x-chip devices on source wafer with sacrificial layer and tether system



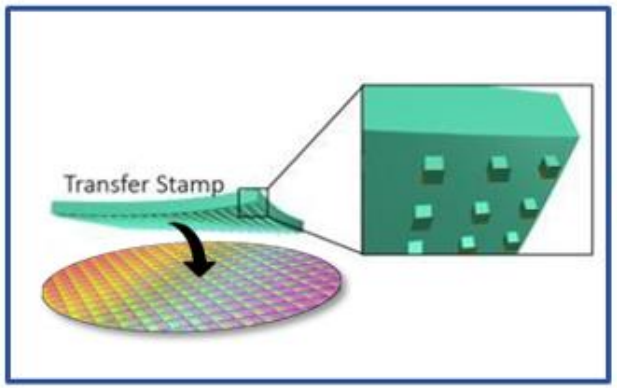
Step 2: Create custom tailored stamp to transfer devices



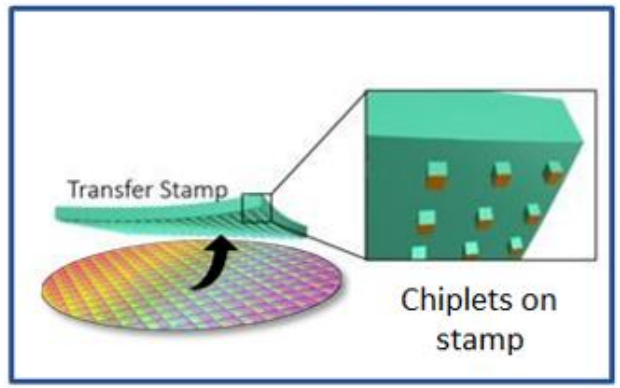
Step 3: Chemical etch to sacrificial layer on source wafer, creating suspended devices



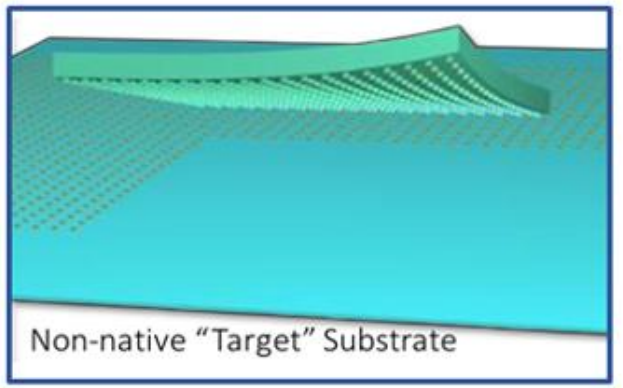
Step 4: Align stamp with devices to be transferred



Step 5: Lift stamp and break tethers, removing devices



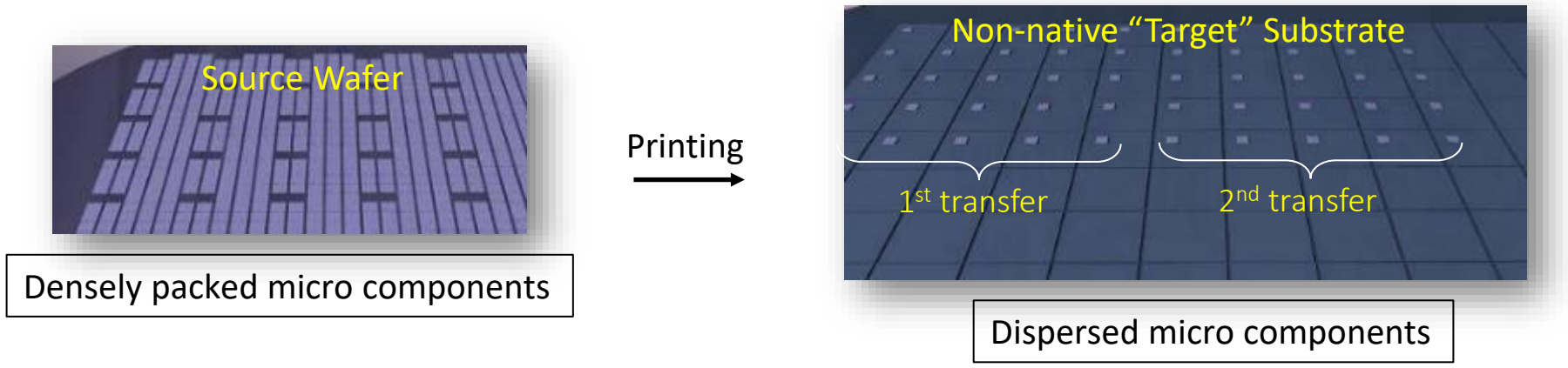
Step 6: Stamp contacts target wafer and transfers devices



Repeat for as many devices or designs as desired

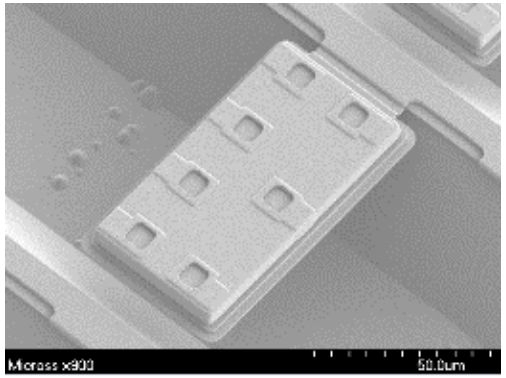
MTP Technology Attributes

- Manipulate objects that are too small, numerous, fragile, or otherwise difficult to handle by other means
- Massively parallel high-throughput micro-assembly
- Decouples growth (high temp, lattice constraints) and usage (glass, plastic, ceramic) of high-performance materials
- Tolerant to wafer-size mismatch
- Uses device source wafer efficiently
- Printing tool scales to large-format target substrates, suitable for high-volume manufacturing
- Effective for “area multiplication” (geometric magnification)



What is Needed for MTP?

Release-Ready Source Material

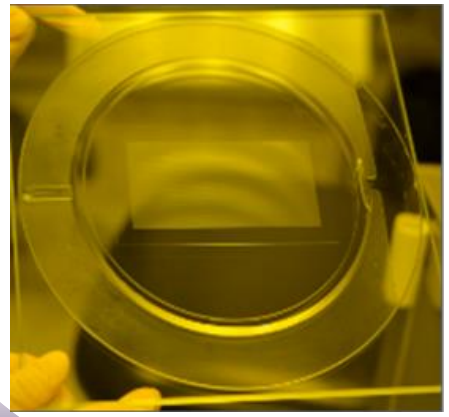


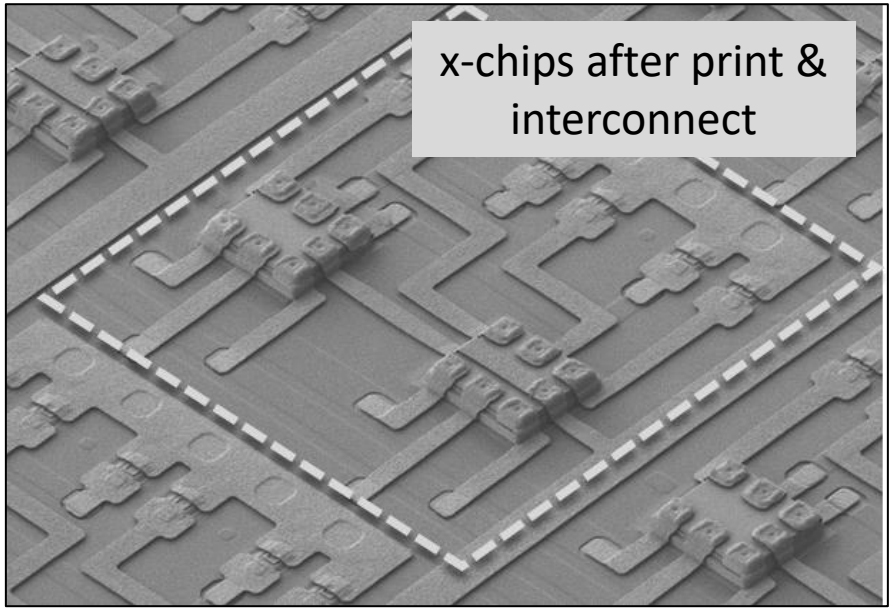
Four main components are needed to enable MTP and create an interconnected solution

- Release-ready x-chip wafer
- MTP Stamp
- MTP Print Tool
- Target wafer / substrate

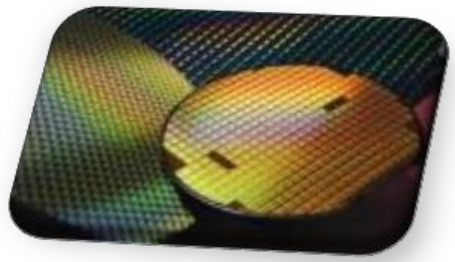
MTP Print Tool

MTP Stamp

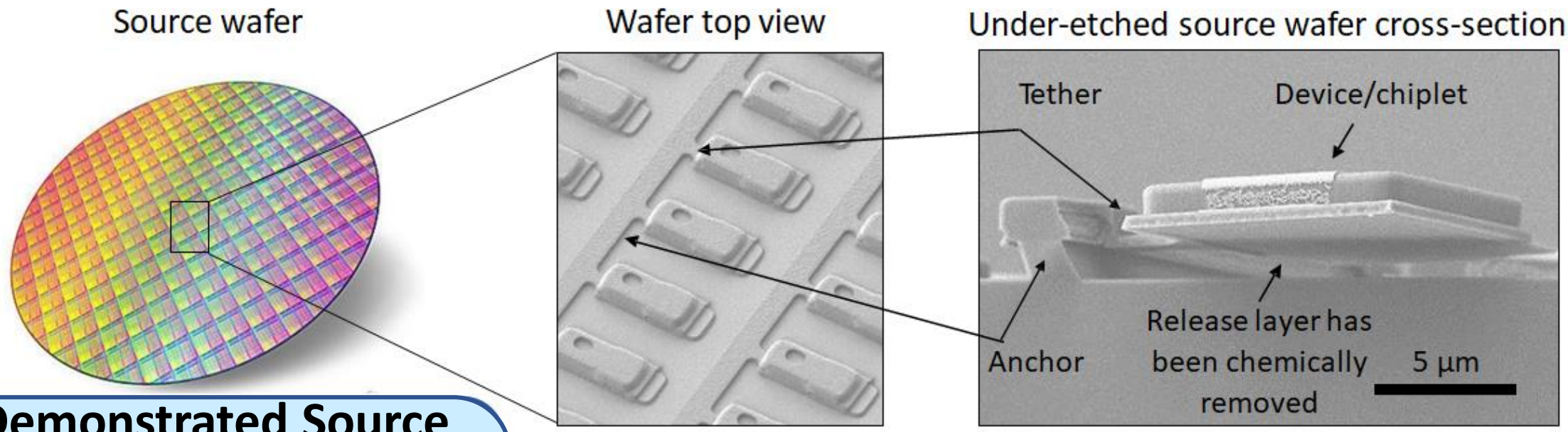




Target Wafer / Substrate



X-chip Source Wafer Fabrication



Demonstrated Source Materials

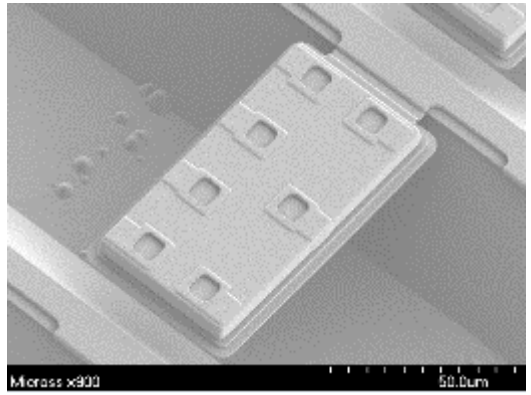
- Si CMOS on SOI
- InP Optoelectronics
- GaAs Transistors
- GaN RF components
- GaAs Lasers

Fabrication:

- X-Celeprint partners with X-Fab to use the XT018 SOI process print ready
- X-Celeprint works with other partners to develop similar SOI and III-V capabilities
- X-Celeprint offers prototyping for print-ready source wafers in both North Carolina and Cork Ireland
- X-Celeprint provides technology transfer and training for customers and customer partners

Methods to Create X-Chips

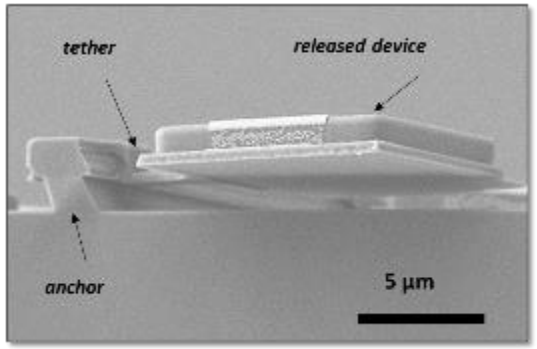
SOI x-chips



SOI undercut with TMAH

- Use wafer with base <100> or <111> crystal plane orientation
- Remove silicon under x-chips with TMAH or KOH
  Oxide under x-chips acts as a barrier against etch of x-chips above

III-V x-chips



GaN on Silicon LED undercut with TMAH

- If III-V material is grown on silicon <100> or <111> substrate, a TMAH etches silicon underneath x-chips while not etching III-V material

Substrate	Release Layer	Release Agent
Silicon on Insulator (SOI)	Buried Oxide (BOX) of SOI	HF (conc.)
GaAs	AlGaAs	HF or HCl
Si (111)	Si (111)	KOH or TMAH (hot)
GaAs	InAlP	HCl
InP	InGa(Al)As	FeCl3 or H3PO4:H2O2 or citric acid: peroxide
InP (InGaAs)	InP	HCl
Silicon on Insulator (SOI)	Si (100)	KOH or TMAH (hot)

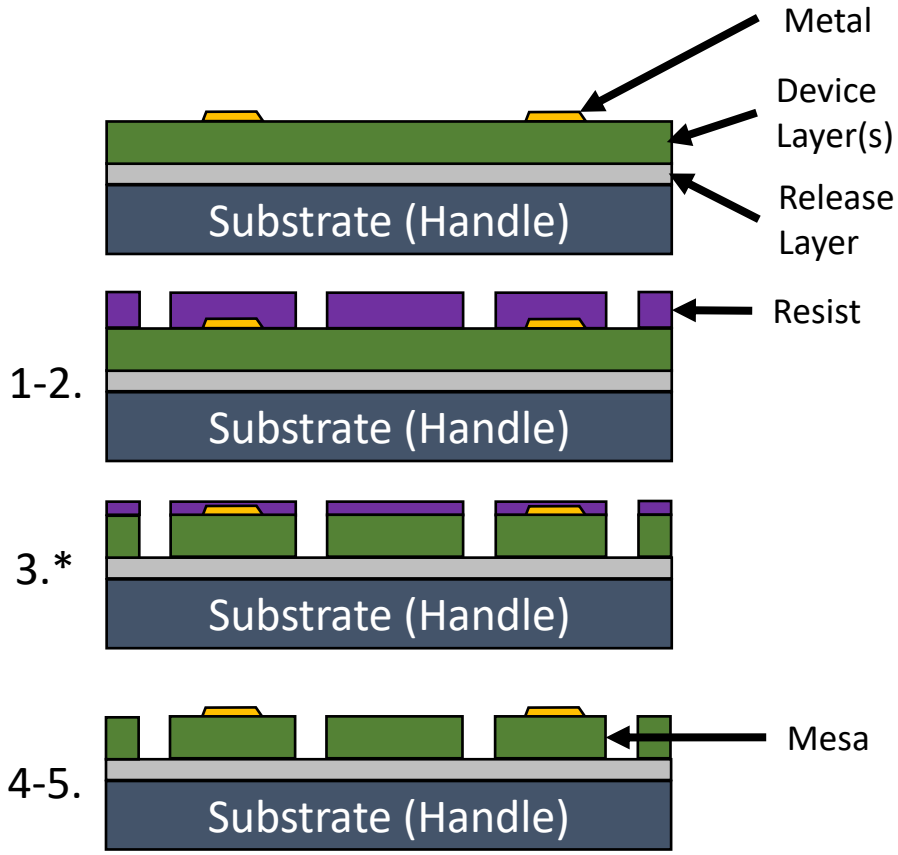
Table of Release systems

Device Singulation/Definition

Singulate devices by etching through the device layer(s) and landing on the release layer.

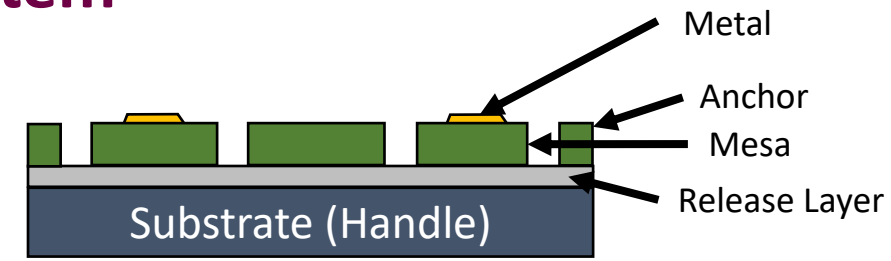
Dry Chemistry

1. Coat and Pattern Wafer
2. Descum
3. Dry Etch in RIE to Release Layer
4. Strip Photoresist
5. Descum



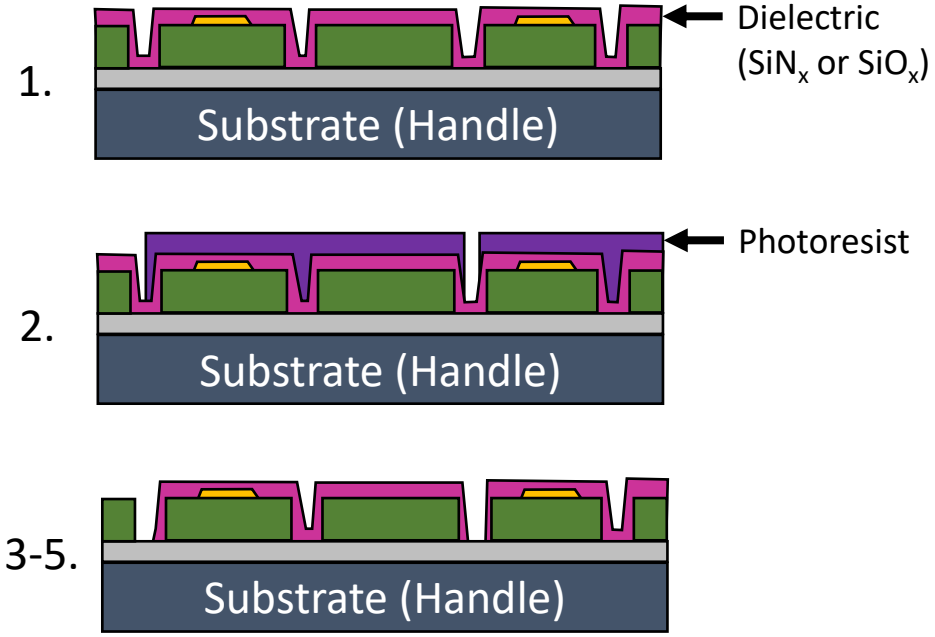
* For photoresist tethers, the etch will land on the handle rather than the release layer.

Create Anchor-Tether System



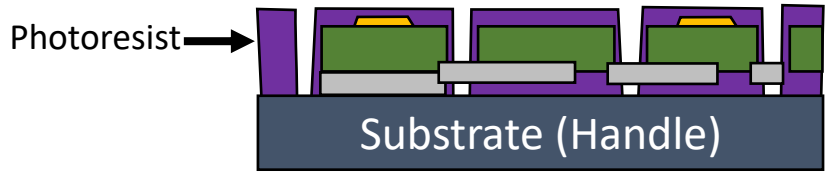
Process 1
Dielectric Tether

1. Blanket Coat Dielectric
2. Coat and Pattern Photoresist for A-T System
3. Dry Etch
4. Strip Photoresist
5. Descum



Process 2
Photoresist Tether

1. Coat and Pattern Wafer
2. Coat and Pattern Wafer

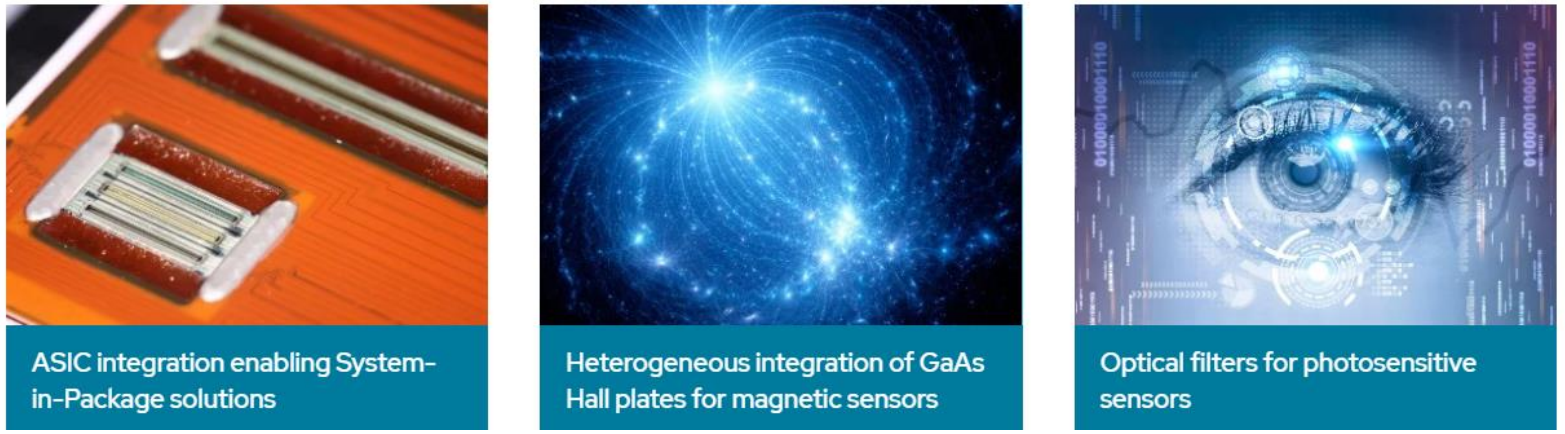


Generally, the tether surrounds the device on all sides, and inlets to the release layer are patterned

X-FAB MTP process

Our partner company X-FAB Erfurt has developed a pilot line for MTP

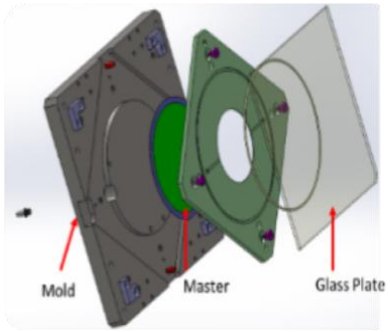
- Industry first pilot line for the integration of smart systems by MTP.
- XFAB is currently integrating Customer Specific projects into their pilot line.
- XFAB and X-Celeprint are currently working to develop a PDK for the XT018 print ready process.

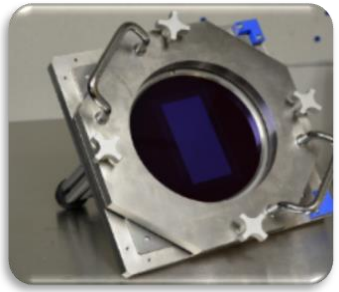


https://www.xfab.com/technology/wlp-3d-int

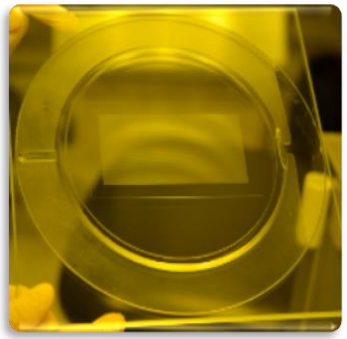
MTP Stamp Construction

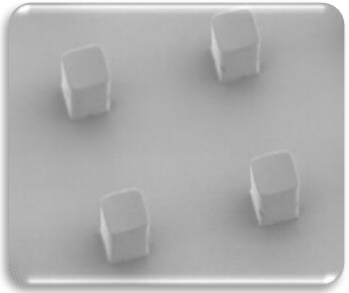
Silicon Master





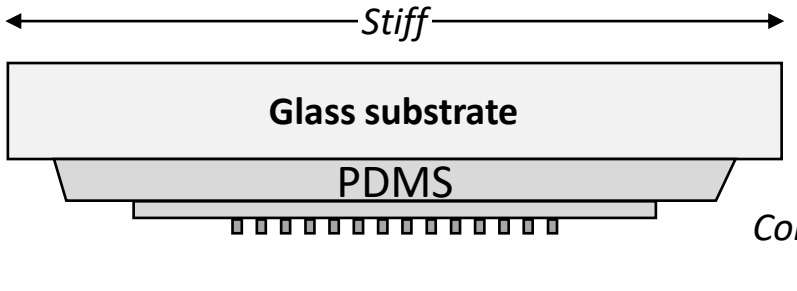
Low-Pressure Injection Molding





Elastomer Stamp

Compliant elastomer (PDMS) material with soft posts on stiff glass substrate

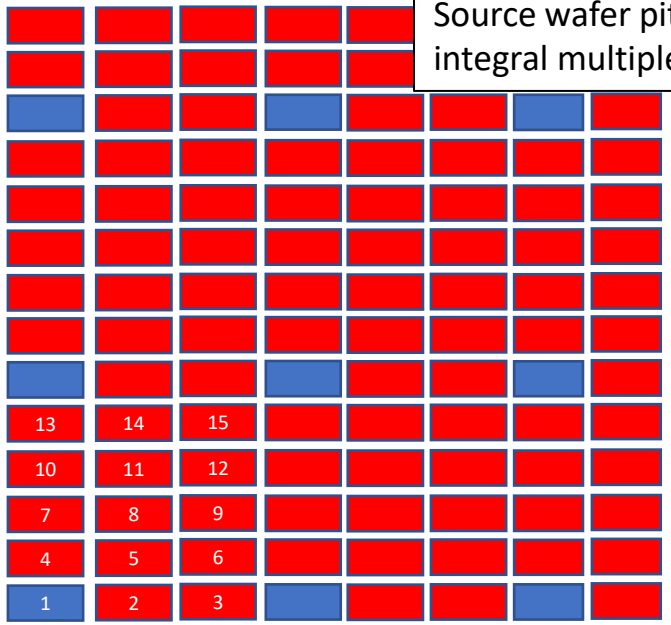


Custom post size and spacing
For desired x-chip placement on destination substrate

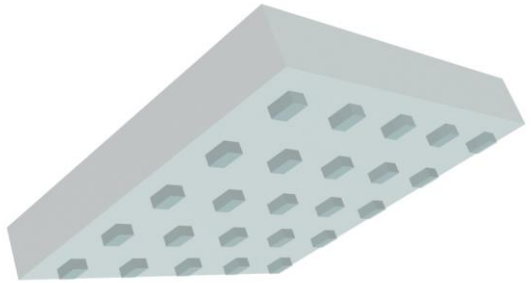
MTP stamp
Close-up for one die

1. A stamp master is fabricated in silicon with standard fab photo processes
2. PDMS is cast between the stamp master and a sheet of glass in a glass mold.
3. The assembly is cured and the glass and PDMS are separated from the stamp master.

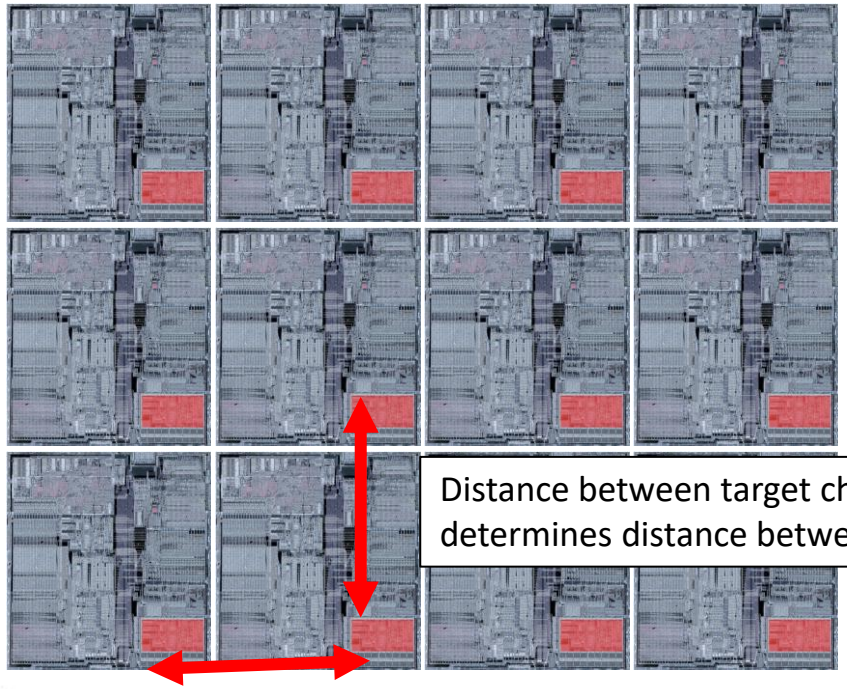
Geometric Magnification



Source wafer pitch matches an integral multiples of the target wafer



$$\text{Number of Picks (X/Y)} = \frac{\text{Distance between stamp posts (X/Y)}}{\text{Distance between printable objects on source(X/Y)}}$$



Distance between target chips x/y determines distance between posts

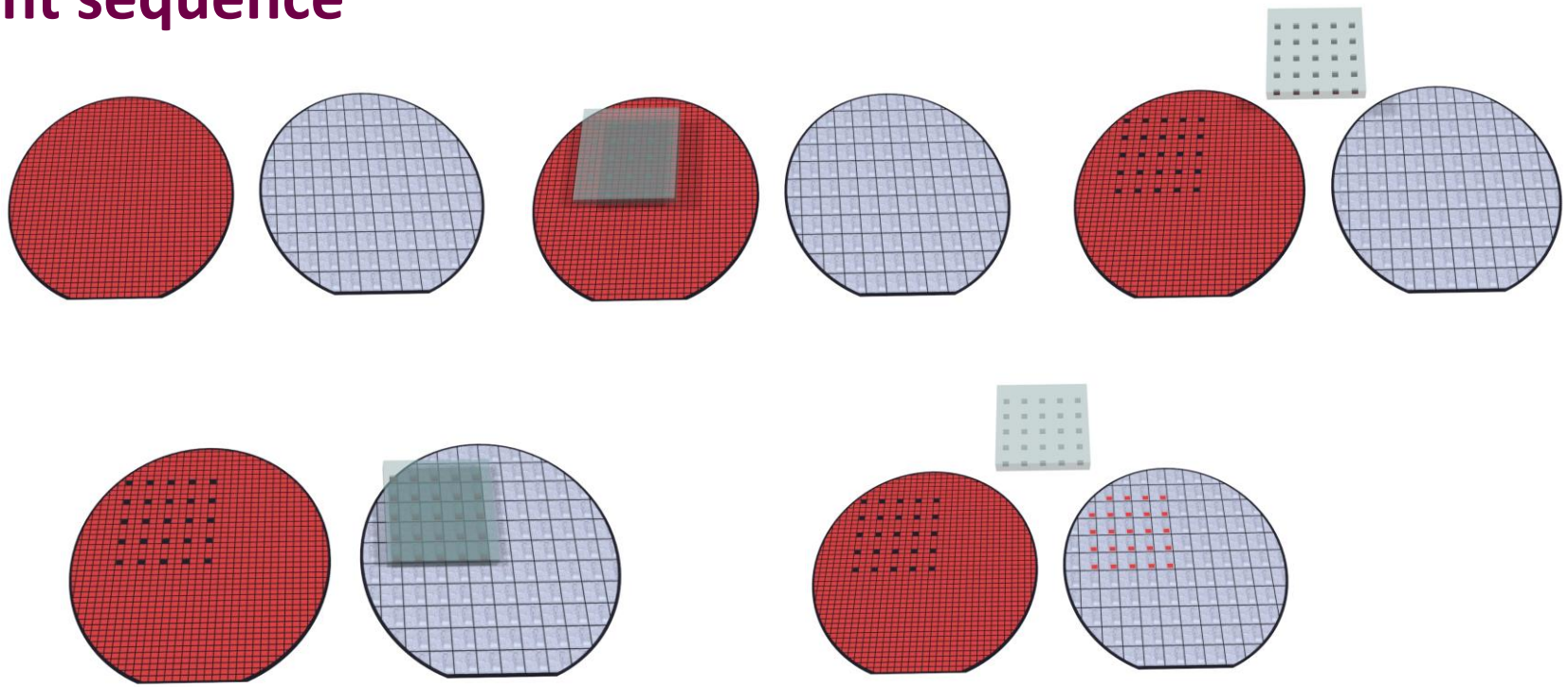
Source Substrate

Target Substrate

$$\text{Total Number of Indexes} = \text{Number of Picks (X)} * \text{Number of Picks (Y)}$$

- Devices can be fabricated at any foundry on the device's native substrate and can be densely packed.
- A custom stamp matches the pitch of the receiving substrate in X and Y dimension.
- X-chips are spaced on a source wafer with a pitch matching a target substrate spacing.
  - In the example above, every third x-Chip in the X dimension and every fifth x-Chip in the Y dimension are printed at a time.
  - 15 separate prints steps transfer all of the x-Chips.

First Print sequence

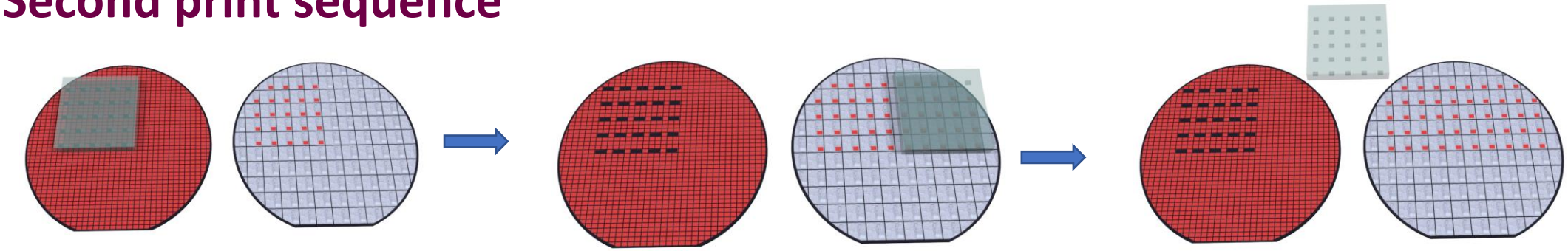


- Stamp posts adhere to x-chips via van der Waals force
- Stamp visco-elastic behavior* enables:
  - Fast separation speed in pick-up regime
  - Slow separation speed in printing regime
- Lifting stamp breaks tethers and removes x-chips
- Massively parallel selective pick-up and transfer of thousands of x-chips
- Readily transfers ultra-thin x-chips

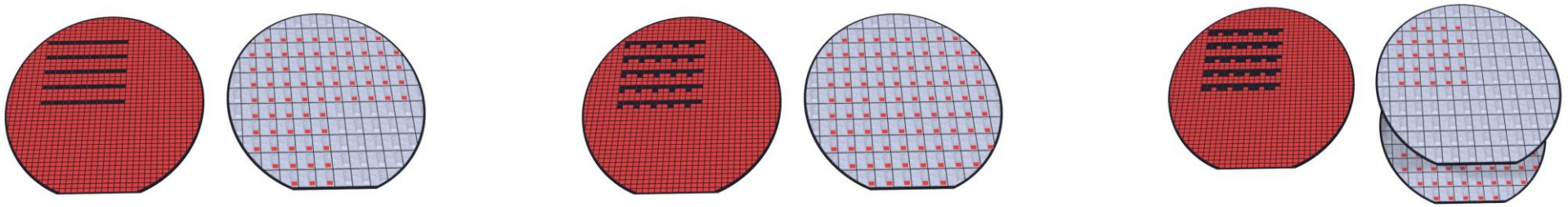
- Stamp contacts destination substrate and x-Chips stick to new surface
- X-Chips placed with controllable pitch and pattern
- A relative “slow” separation speed is used in the 10s of um range to print the x-Chip to the substrate.

*Meitl, M. A., Zhu, Z.-T., Kumar, V., Lee, K. J., Feng, X., Huang, Y. Y., … Rogers, J. A. (2006). Transfer printing by kinetic control of adhesion to an elastomeric stamp. Nature Materials, 5(1), 33–38. https://doi.org/10.1038/nmat1532

Second print sequence

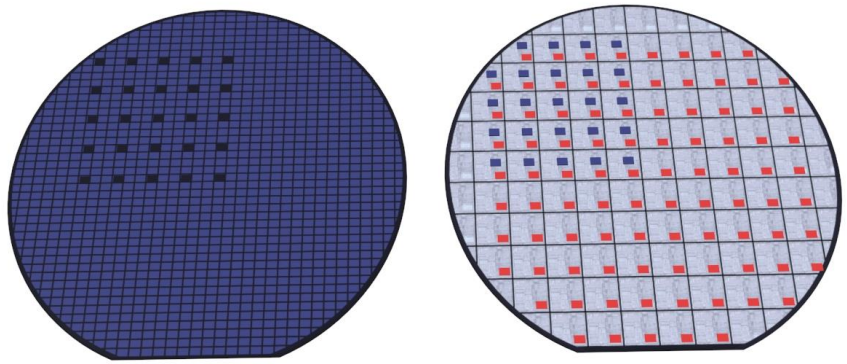


Third, Fourth and Fifth Prints – Note fifth print starts new destination wafer



First print of second type of x-Chip on previously printed wafer

- MTP enables a variety of x-Chips to be printed on the same target wafer.
- The x-Chips can be of the same material type or a different material type.
- Different x-Chips can perform a different function, i.e., one x-Chip could be a laser, while another could be a sensor.

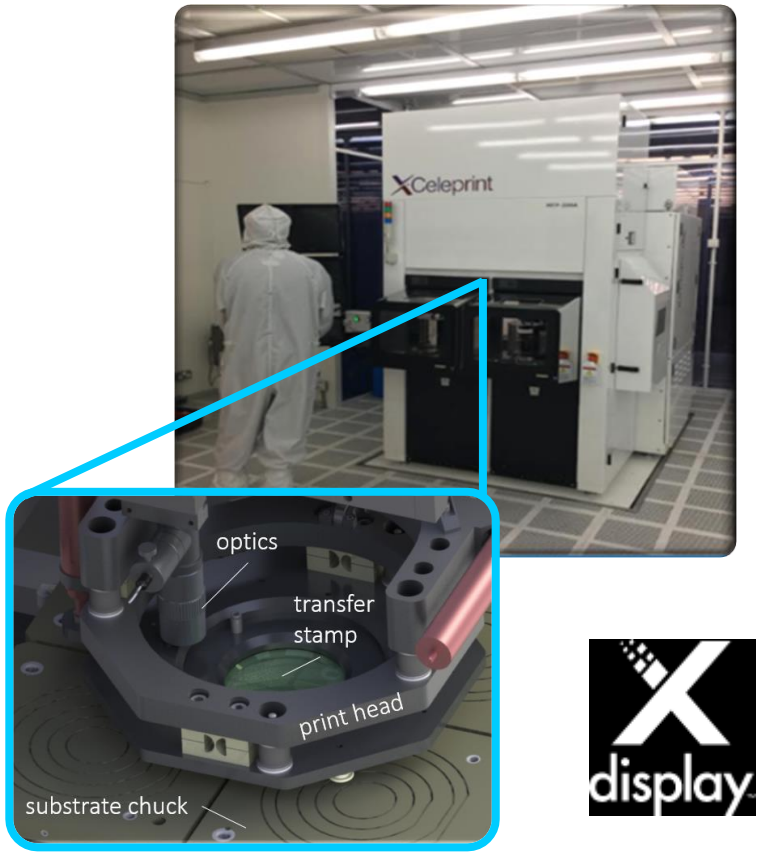


MTP Print Tool

- Currently there are two companies producing print tools:
  - X Display Company
  - ASM/Amicra

- All print tools are built to provide:
  - Robust, automated toolset for mass-transfer including proprietary stamp, motion platform, and optics for precision alignment.
    - MES (manufacturing execution system) interfaceable
    - Demonstrated >15,000 transfer cycles per stamp
  - CMOS fab-compatibility
  - 200 - 300 mm capability

- Gen 4.5 Panel print tools under development



Fully automated 200mm tool offered by X Display Company

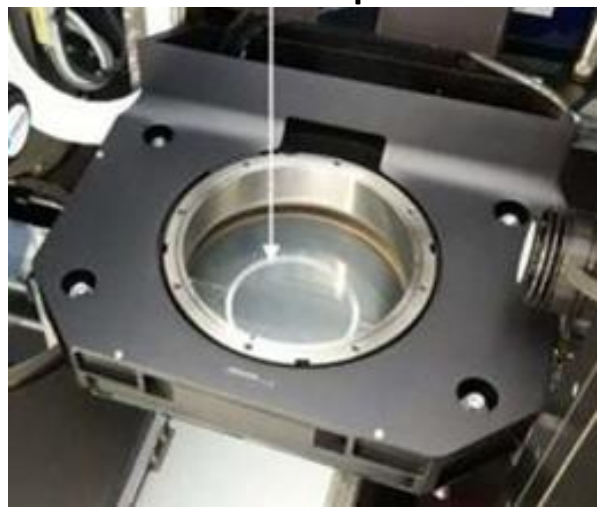
Nova+ MTP Manufacturing System

Features

- Fully automatic high-volume manufacturing system
- ISO 4 clean room class
- Up to 300x300mm source wafer
- Up to 450x450mm destination substrate (wafer or panel)
- 50x50mm (max) stamp array
- ~40 sec cycle time for 1 stamp transfer with 2-point alignment
- ± 1.5µm @ 3σ placement accuracy
- Dual bond head system
- Look-through bond head
- Automatic tip-tilt adjustment

Nova+ MTP Manufacturing System

MTP Stamp



Additional ASM AMICRA MTP Systems	▪ AFC+ for R&D and low volume manufacturing ▪ NANO: ± 0.5µm @ 3σ placement accuracy ~40-65 sec cycle time, 20x20mm (max) stamp array

Contact Johann Weinhändler: Johann.Weinhaendler@asmpt.com

Micro Transfer Printing in Action

Printing an array of 20x28 devices onto a silicon target substrate

Objective field of view shows 1 field.

1. *pick-up,*
2. *print,*
3. *clean.*

[repeat]

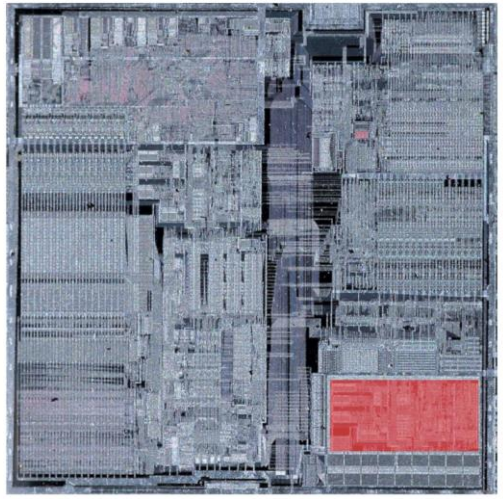
Play Video

MTP Target Substrate

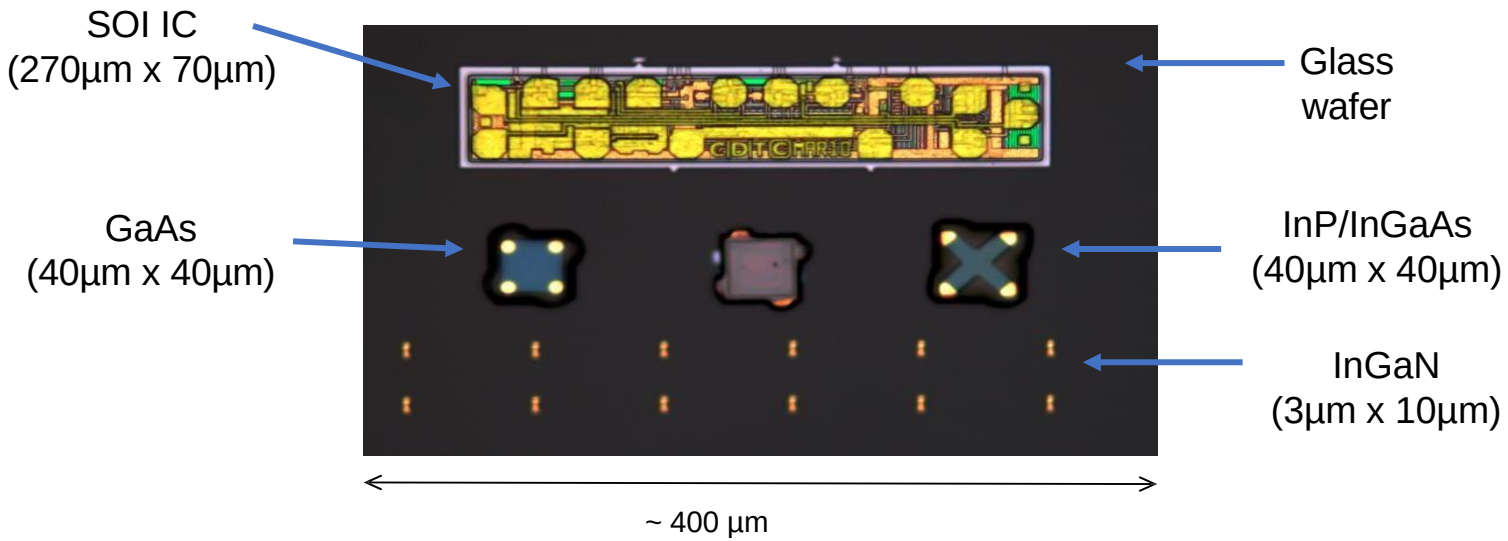
- MTP target substrates can be a variety of materials (Si, glass, plastic, ceramic) and surfaces (smooth, rough etc.)
- Target use is dependent on the application.
  - x-chip onto 2.5D interposer (Heterogeneous Integration)
  - x-chip onto silicon device wafer (chip-on-chip) i.e., 3D

Demonstrated Target Substrates

- Silicon CMOS
- Glass
- Plastic
- Ceramic
- Smooth surfaces
- Rough surfaces
- Non-planar



x-Chip on IC wafer
Chip-on-chip 3D



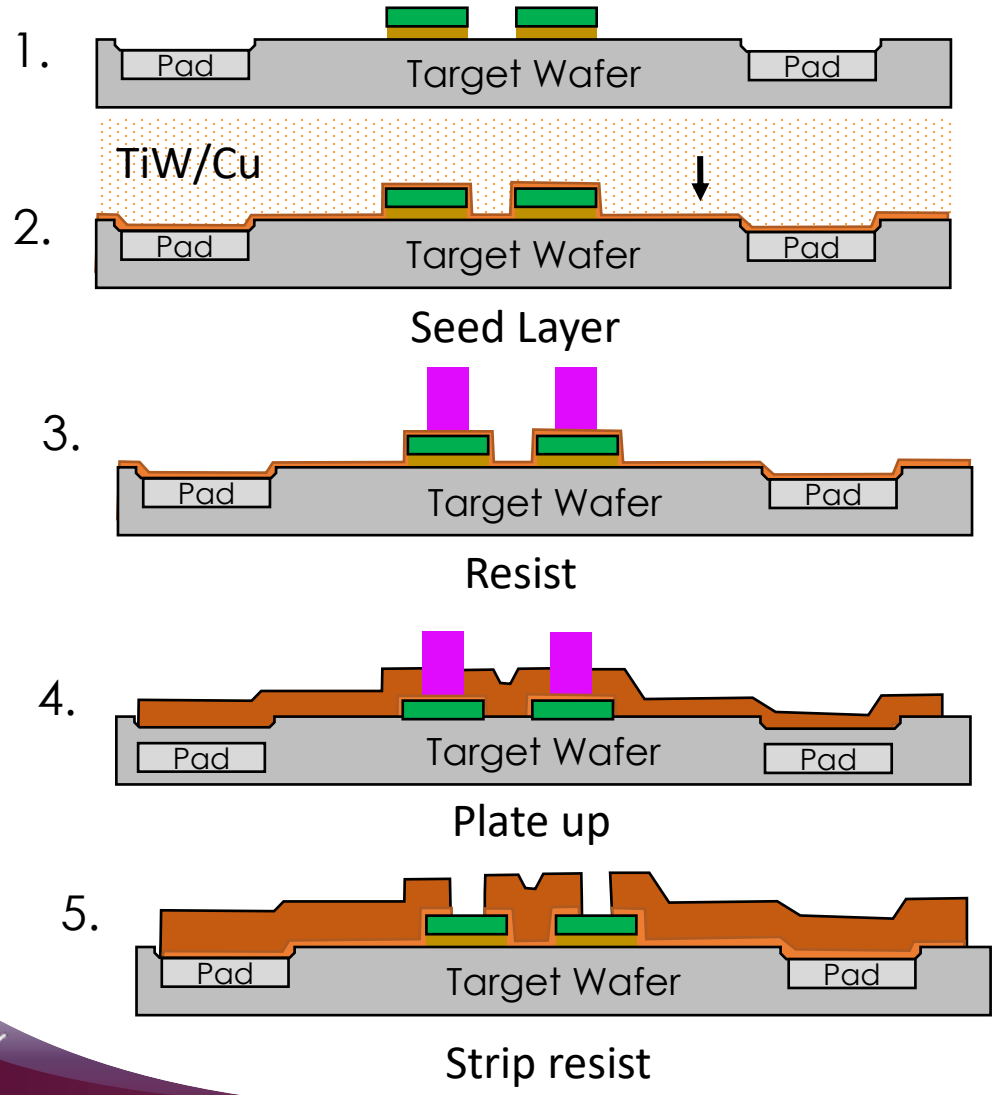
x-Chips for Heterogeneous Integration, i.e., 2.5D interposer

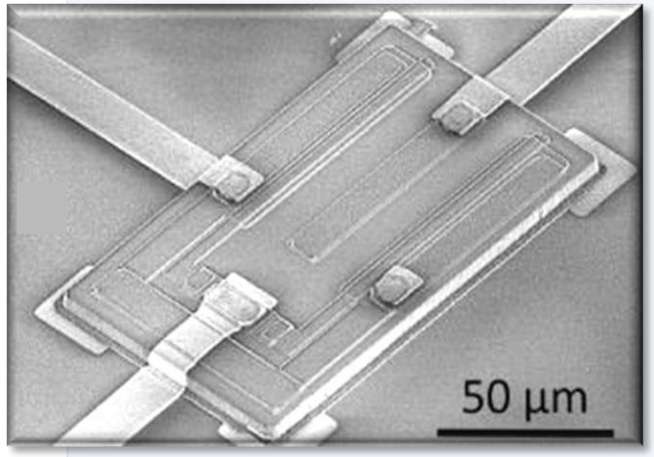
- Printable devices can be made in many important technologies
  - Gallium Arsenide, Gallium Nitride, Indium Phosphide and Silicon

Ultra-Thin X-Chips Enable Standard Thin Film Interconnect

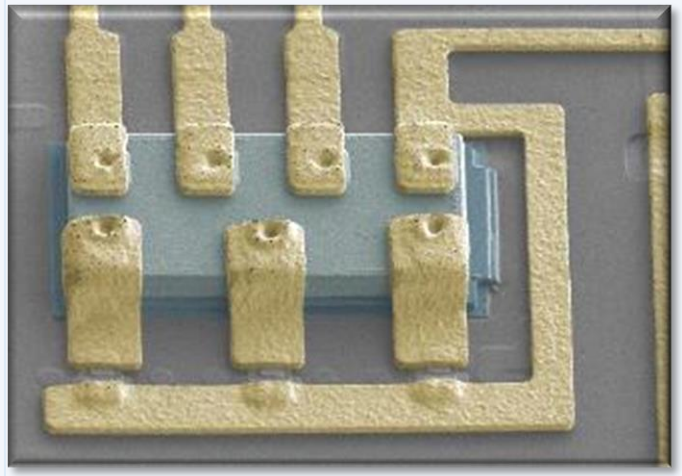
Create seed metal and then electrochemically grow Cu on seed metal where desired to interconnect printed devices with wafer

Printed Devices Ready for TF interconnect

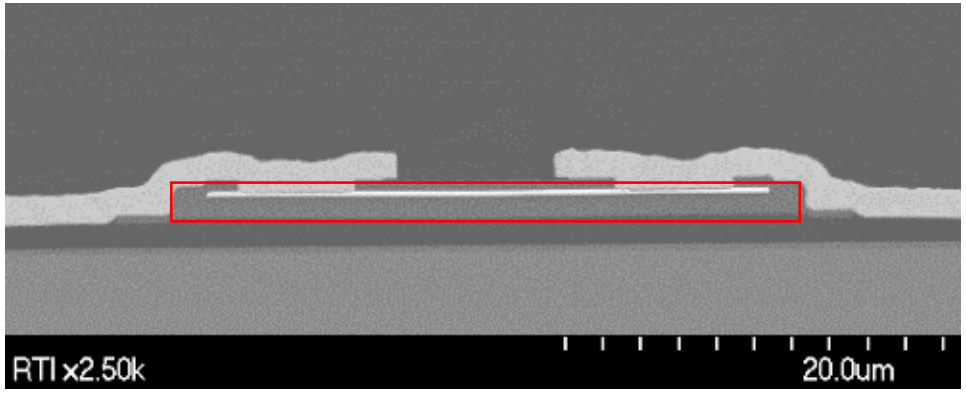




Integration of GaN HEMTs onto Silicon CMOS by Micro Transfer Printing

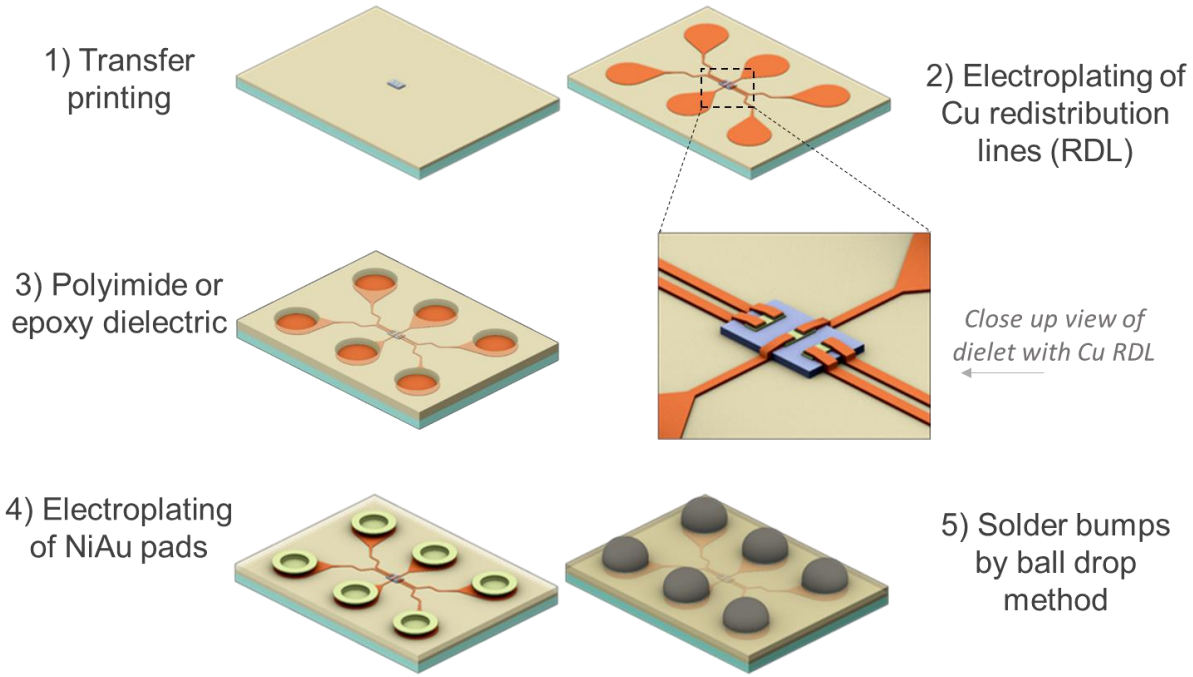


High-Brightness Displays Made with Micro-Transfer Printed Flip-Chip microLEDs



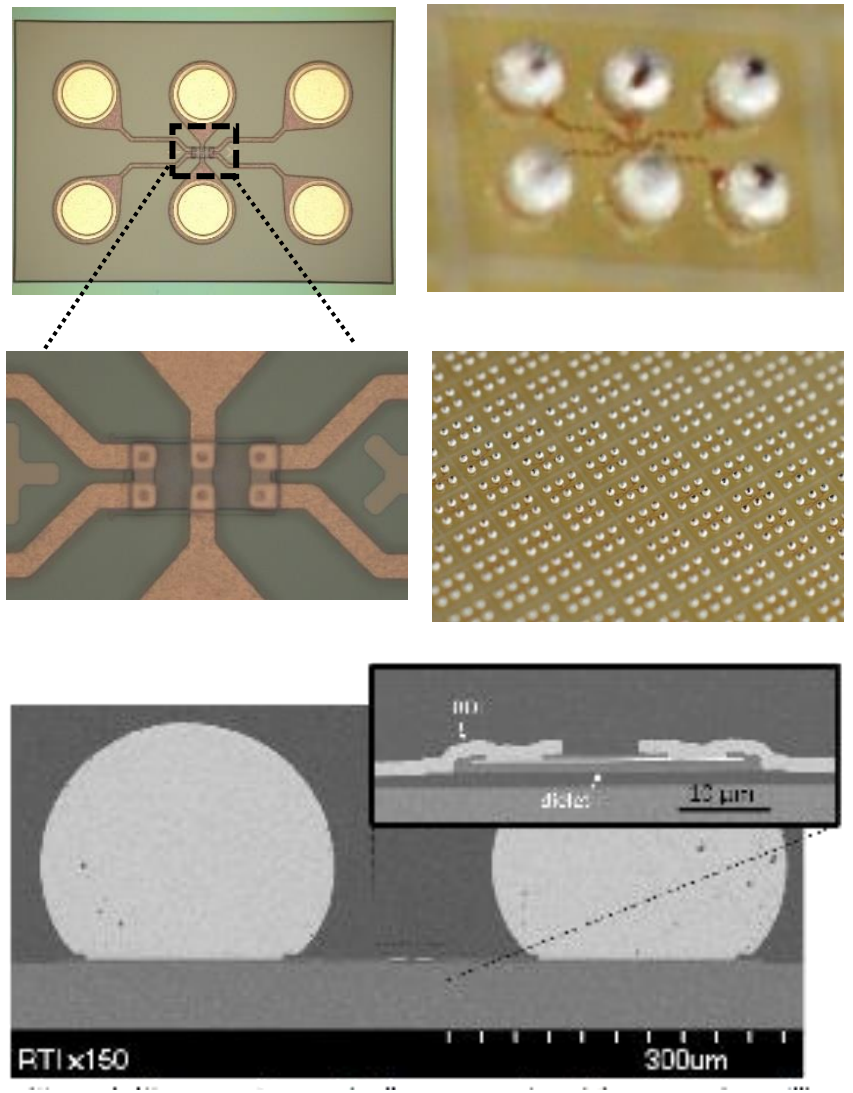
Cross section of micro-transfer printed device

MTP for Bumped Devices & Modules



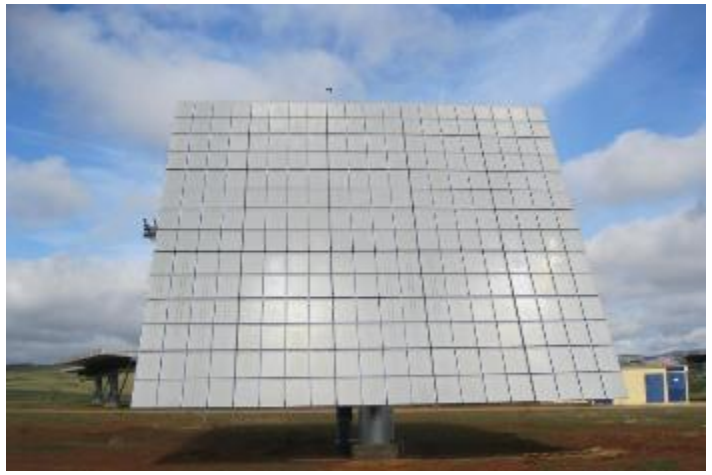
MTP printed devices can be connected and bumped with standard semiconductor processing

Package

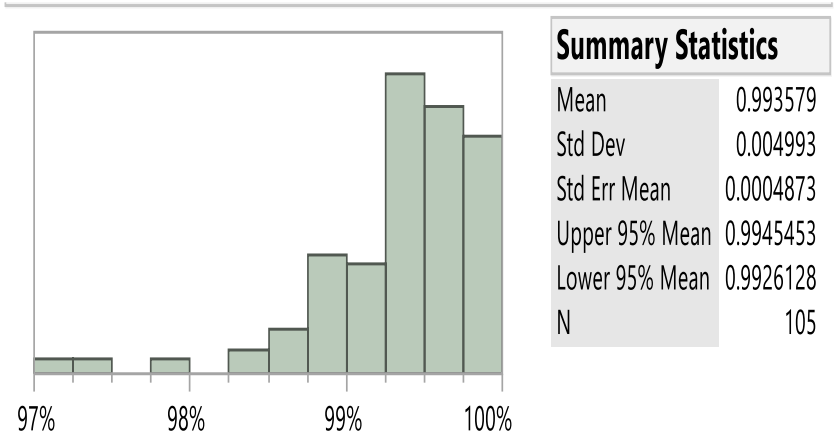


MTP Print Yield for Semprius Solar Cells

- Fabricated surface mountable package with 600 µm, 3J solar cell
- Smaller cell provides competitive advantages in concentrated photovoltaics
- Thousands of target wafers printed in pilot production
- Highly reliable package, >25 billion cell hours in field, passed rigorous reliability testing



24.5 kW CPV system



Summary Statistics	
Mean	0.993579
Std Dev	0.004993
Std Err Mean	0.0004873
Upper 95% Mean	0.9945453
Lower 95% Mean	0.9926128
N	105

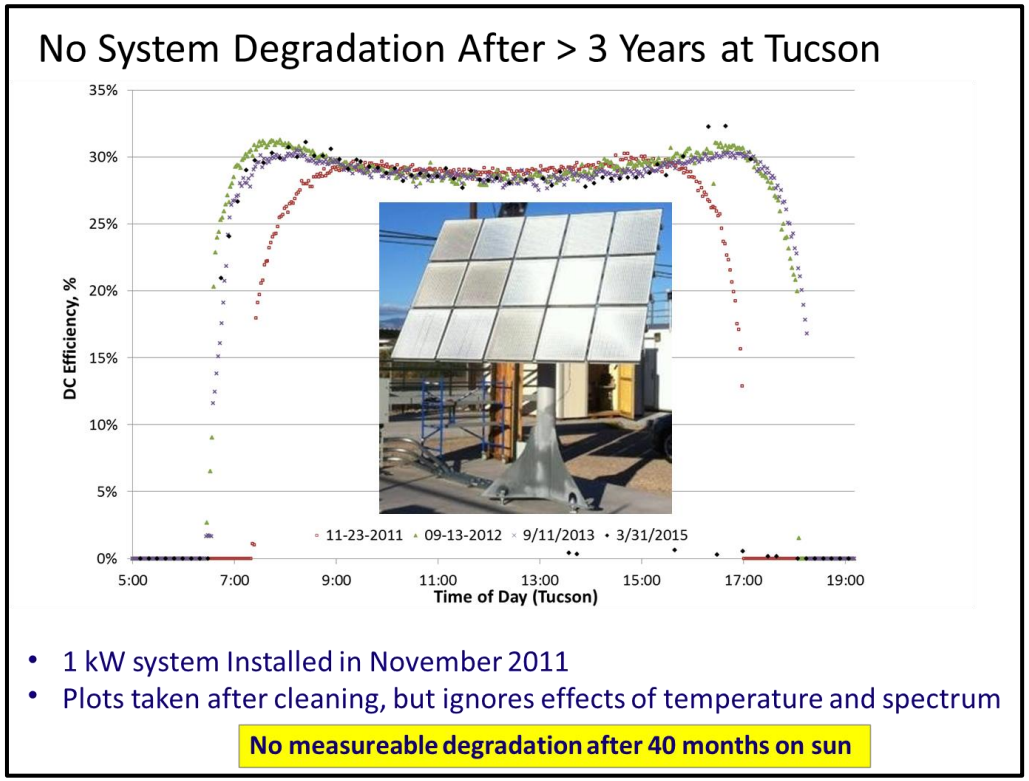
Print Yield Distribution of 105 interposer wafers

150 mm ceramic wafer with 4866 printed solar cells

- Sample of 105 interposer wafers, 4866 die per wafer
- Solar cells printed from 150 mm GaAs wafer to 150 mm ceramic wafer
- Printed with a 24x24 post array stamp, 13 print cycles per target wafer
- Average print yield of 99.3%

MTP Reliability Data

- **Many tests were completed on the Semprius solar modules**
- **These modules consisted of 3J solar cells printed to rough Alumina ceramic wafers with a 3um print adhesive.**
- **All testing showed passing reliability results.**
- **No system degradation was noted at multiple sites. Below is a review of the Tucson Arizona site after more than 3 years.**

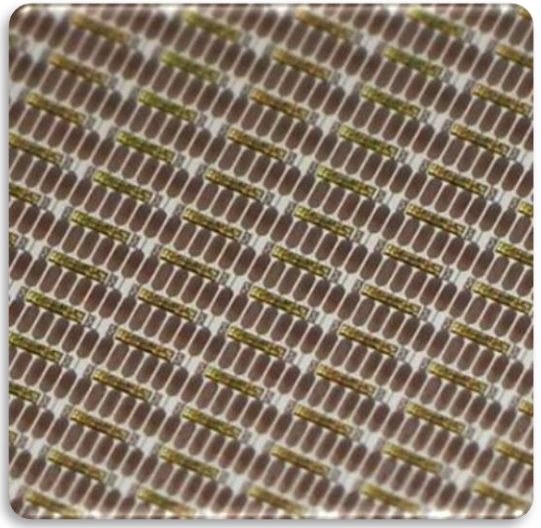


IEC 62108 Testing (as of Jan 2013)		
Section	**Test Description**	**Status**
10.3	Ground Path Continuity	PASS
10.4	Electrical Insulation	PASS
10.5	Wet Insulation	PASS
10.6	Thermal Cycling	PASS
10.7	Damp Heat	PASS
10.8	Humidity Freeze	PASS
10.9	Hail Impact	PASS
10.10	Water Spray	PASS
10.11	Bypass Diode Thermal	PASS
10.12	Robustness of Termination	PASS
10.13	Mechanical Load	PASS
10.14	Off-Axis Beam Damage	PASS
10.15	UV-Conditioning	PASS
10.16	Outdoor Exposure	PASS

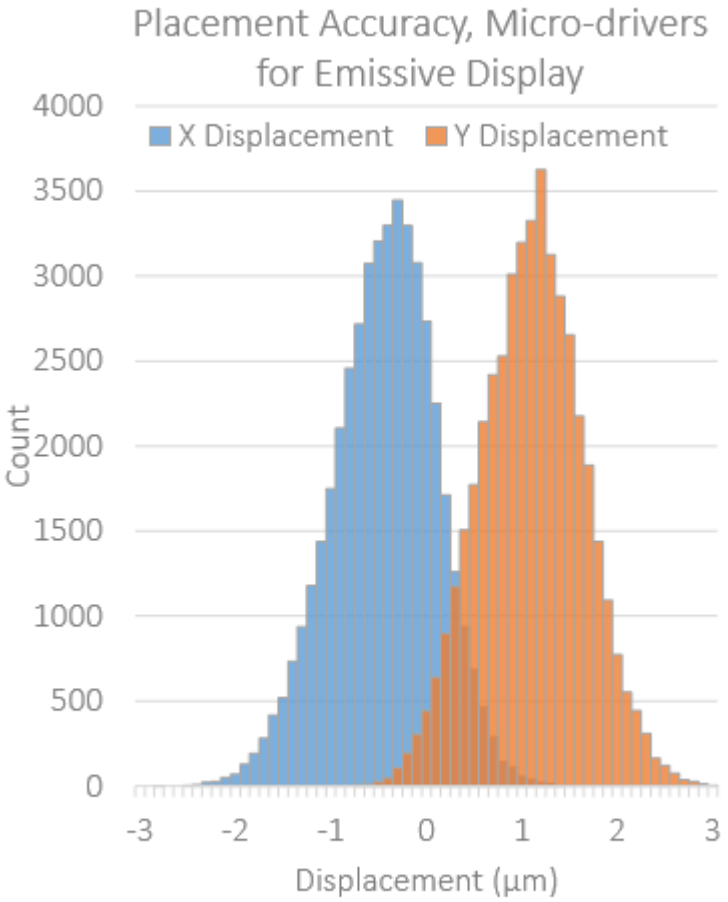
All IEC testing of CPV modules passed

MTP Print Yield – Display Print Drivers on Glass

270x70 µm ICs

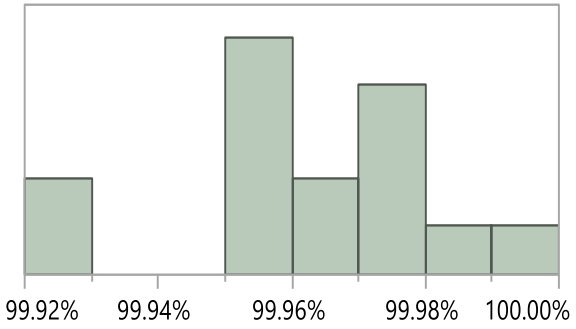


768 µICs per print cycle, 60 print cycles



Displacement distribution of 1 display

Display Print Yield



Summary Statistics	
Mean	0.9995867
Std Dev	0.0001685
Std Err Mean	0.0000435
Upper 95% Mean	0.99968
Lower 95% Mean	0.9994934
N	15

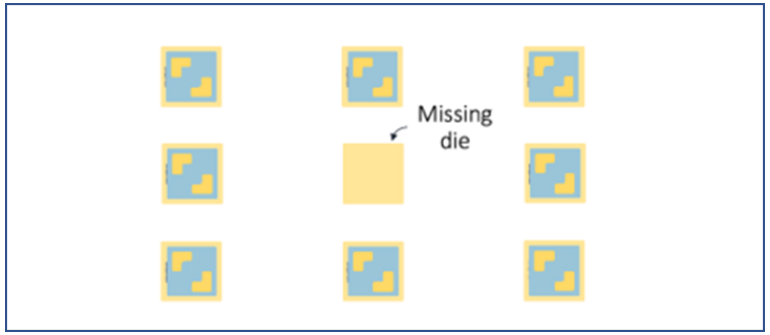
Print yield of 15 displays, each with 46,080 µICs

- 15 displays were made (>690k transferred devices)
- Mean print yield: 99.96%
- Displacement at 3σ: +/- 1.5um

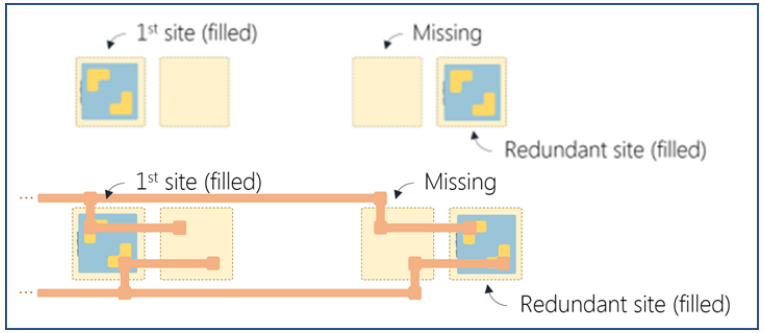
MTP Print Repair

Printing repair can be achieved post printing of the target substrate in multiple ways using a single post stamp to pick-and-print single chips depending on the final yield need.

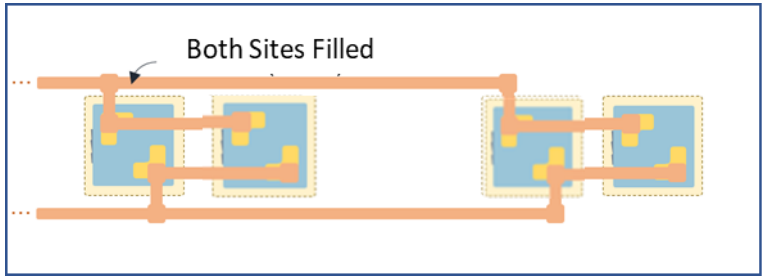
- Printing to a non-printed site with no defects
  - Defect on source prevents x-Chip printing.
  - Defect on the bottom of the x-Chip prevents x-Chip printing



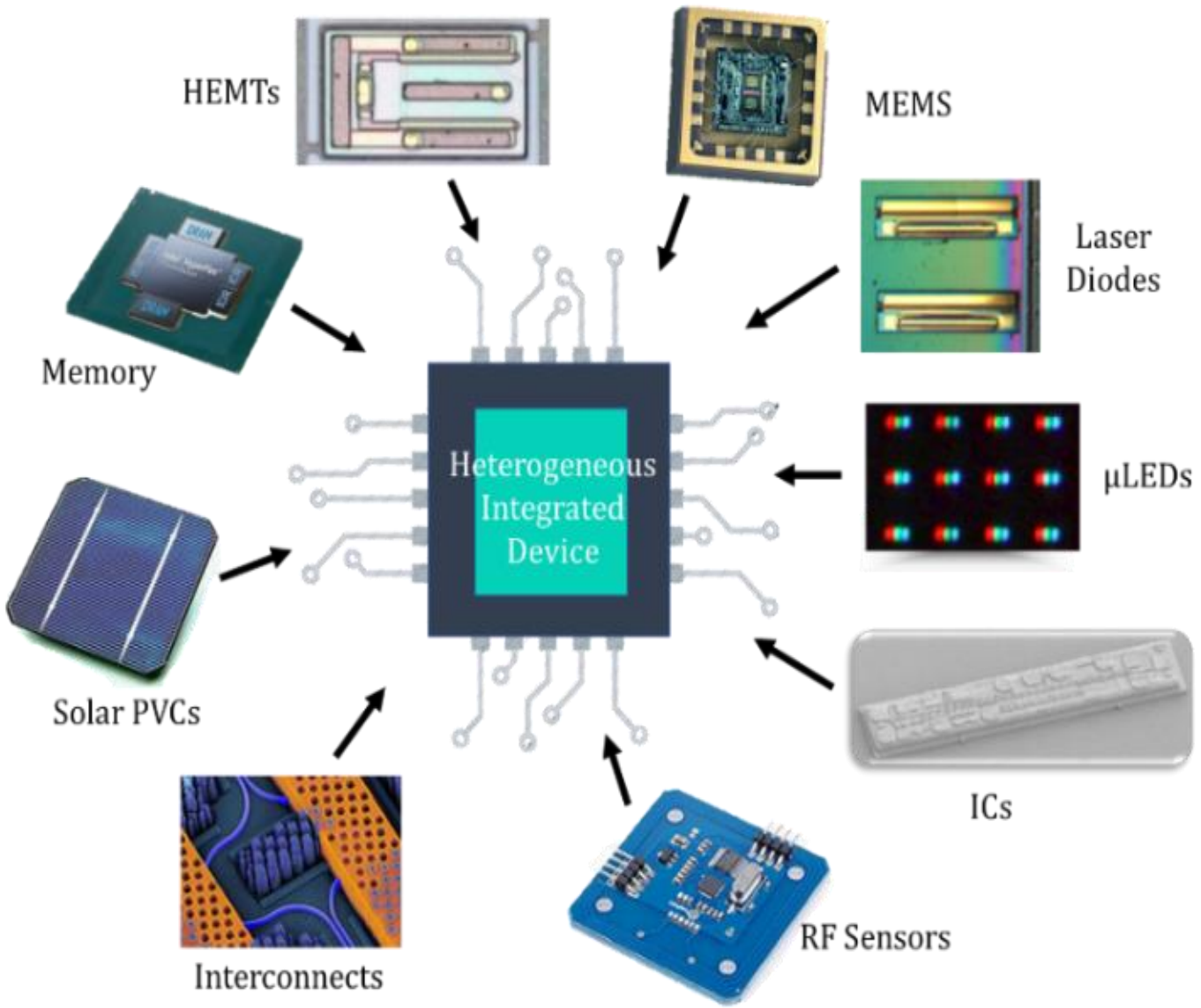
- A second site printing site on target if primary site is defective
  - A defect on the target site prevents printing
  - A defective x-Chip has been printed



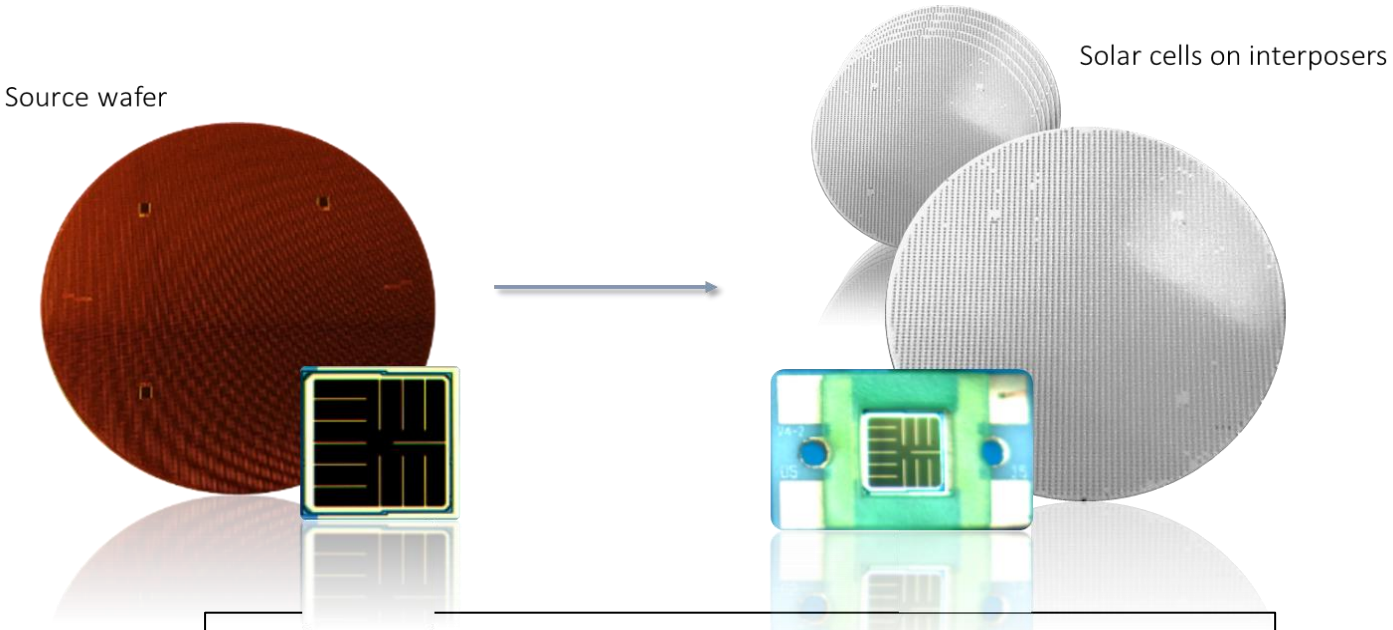
- Redundant device printing compensates for “defective” chips
  - Useful for an application that needs 100% yield



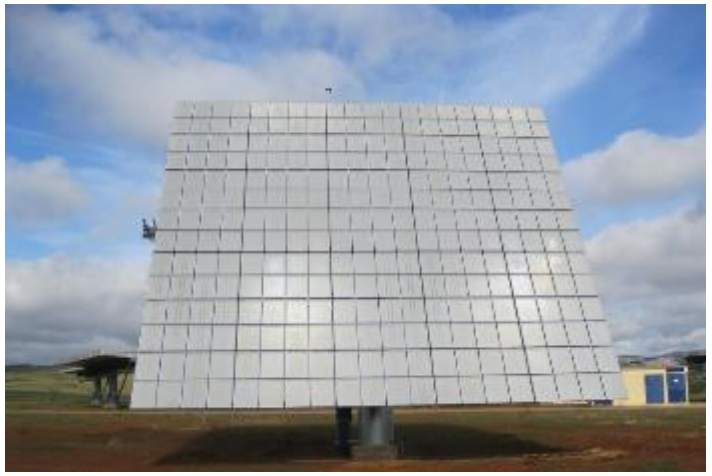
MTP Applications



Printed Multi-junction Solar Cell



150 mm ceramic wafer with 4866 printed solar cells



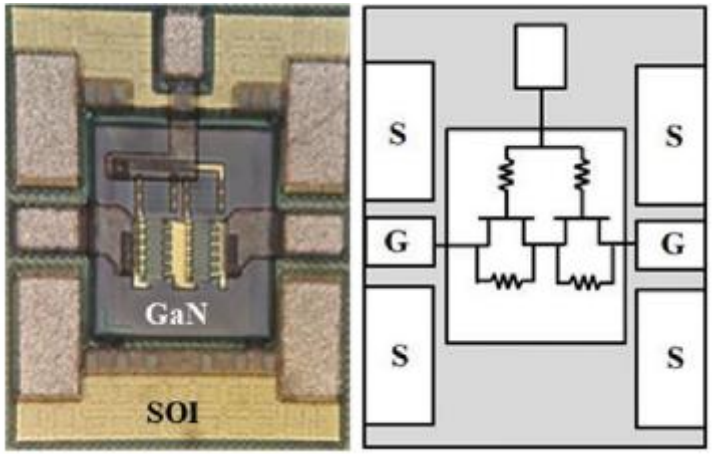
24.5 kW CPV system

module arrays on factory floor, ready for shipping

- Smaller cell provides competitive advantages in concentrated photovoltaics
- 600 µm, 3-junction solar cell uses MTP to fabricate surface-mountable package
- Thousands of target wafers printed to date
- Highly reliable package, >25 billion cell hours in field, passed rigorous chamber testing

RF GaN HEMTs onto Silicon CMOS

- 5G /RF Single Pole Single Throw (SPST) switch of GaN on SOI
- <0.4 dB insertion loss up to 30 GHz
- 59% reduction in vertical capacitive coupling
- Performance attributed to ability of placing GaN on SOI



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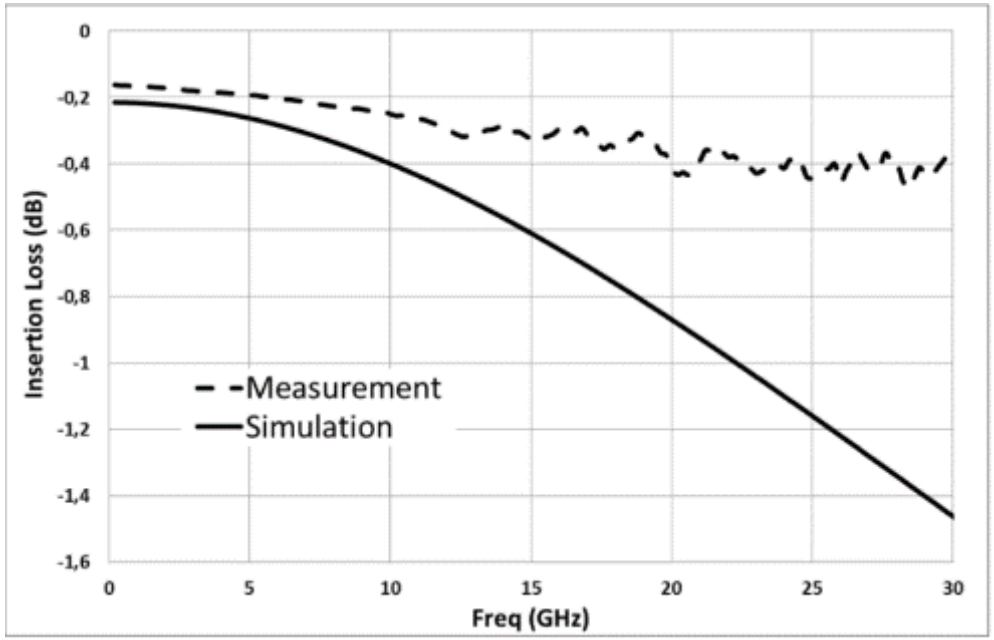

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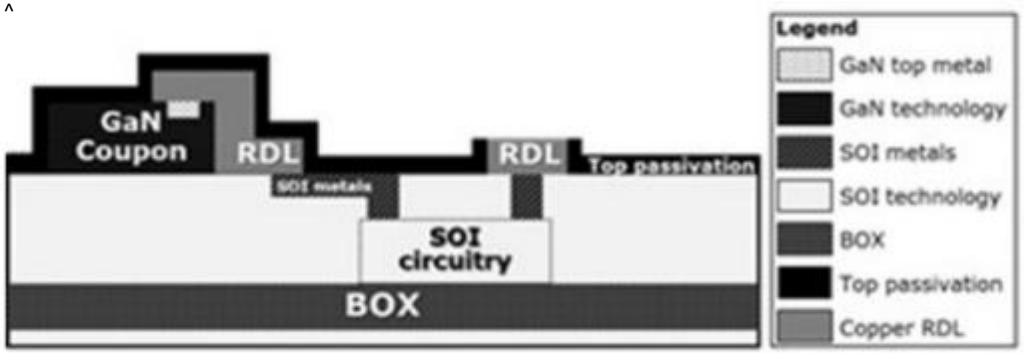
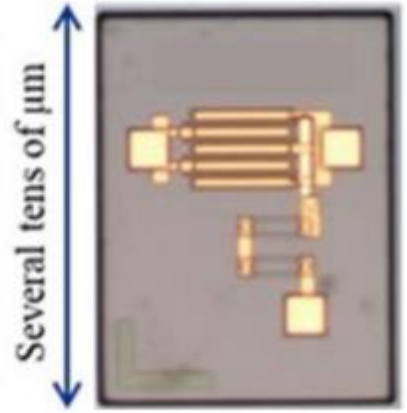




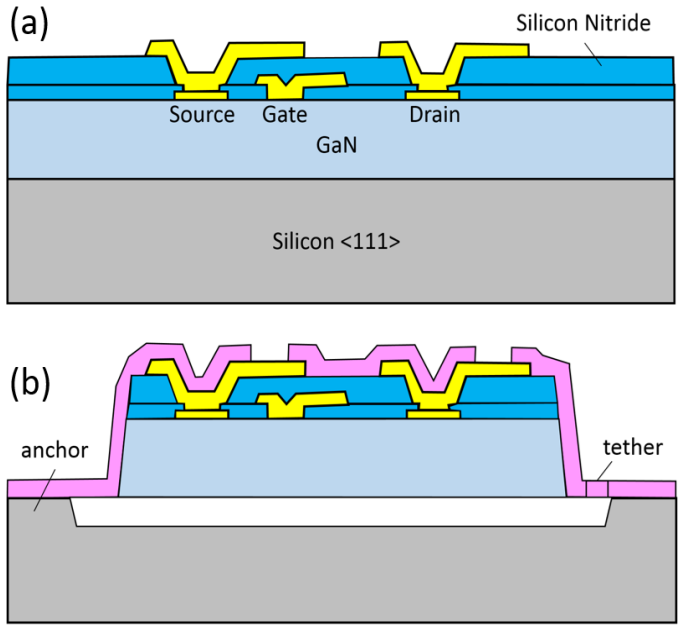
[RF Small and large signal characterization of a 3D integrated GaN/RF-SOI SPST switch]

[RF SPST Switch Based on Innovative Heterogeneous GaN/SOI Integration Technique]

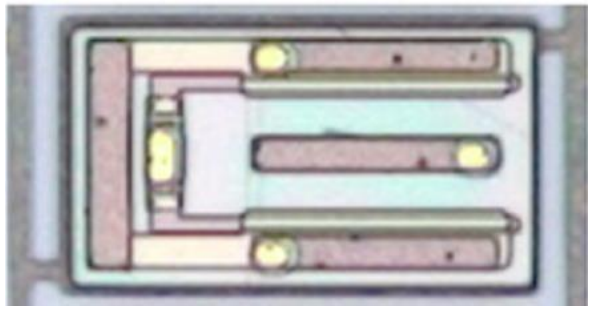
GaN Power Electronics Integrated on CMOS

GaN HEMTs Integrated onto CMOS

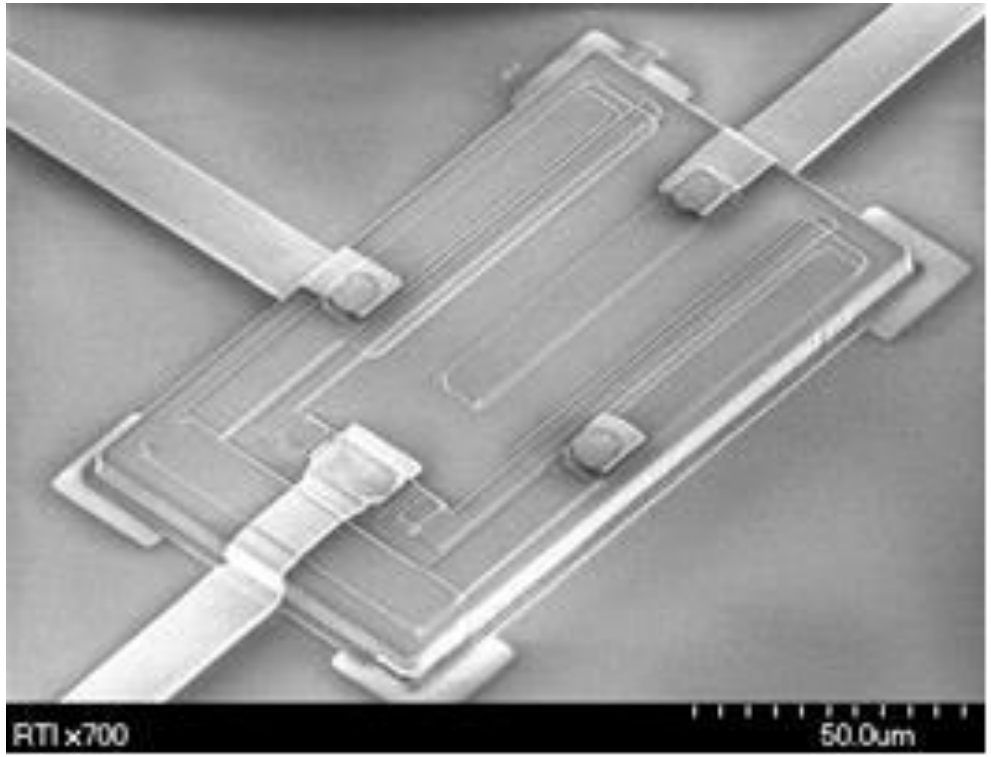
GaN-on-Si Release Process



Ready-to-print GaN HEMT



GaN HEMT printed and interconnected on Si CMOS



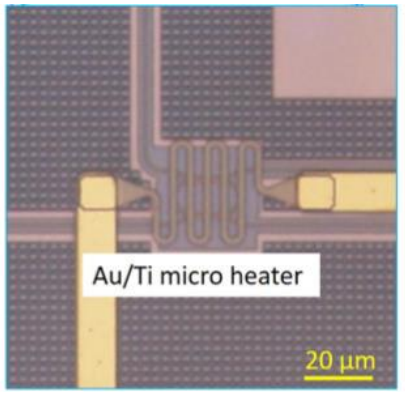
Source

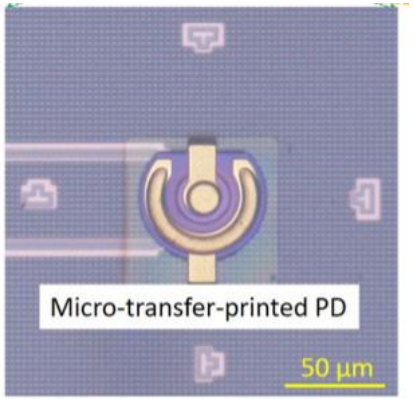
- Integration of GaN HEMTs onto Silicon CMOS by Micro Transfer Printing
- Printing GaN HEMTs onto Silicon CMOS

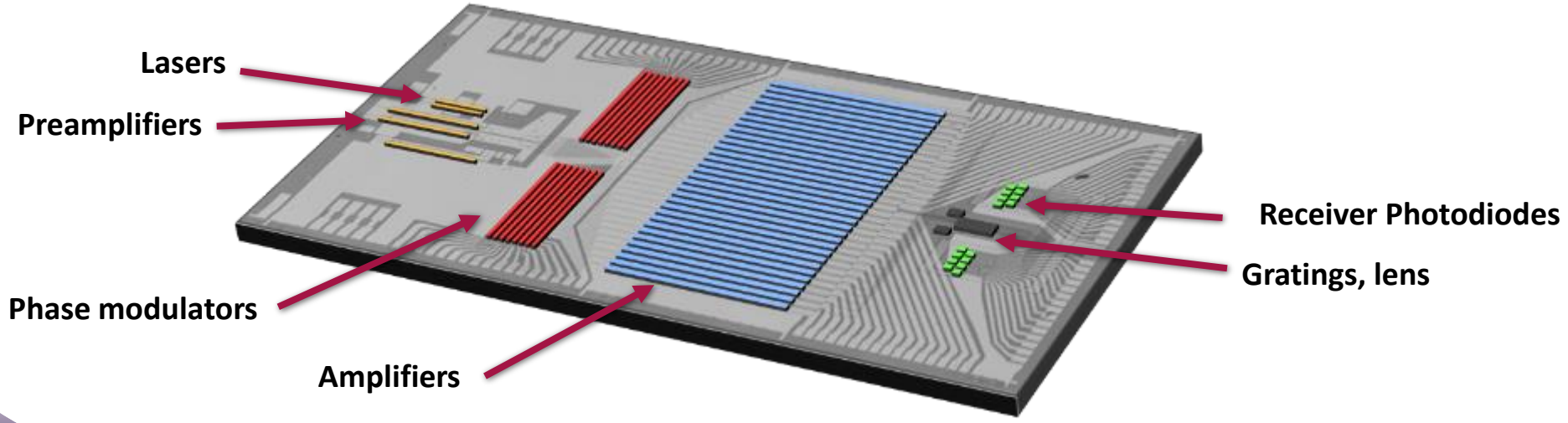
Photonic Integrated Circuit (PIC)

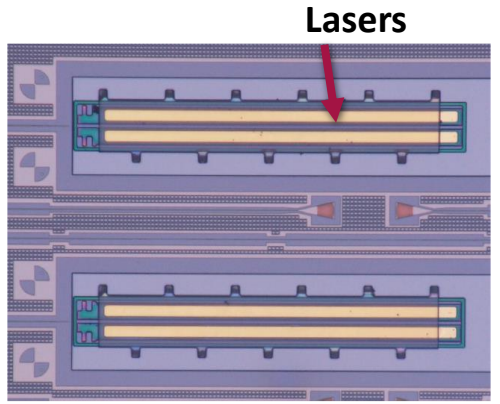
Benefits:

- **Efficient assembly of multiple heterogeneous materials**
  Lasers, modulators, detectors, driver ICs (analog and logic)
- **Precision alignment at each step**
  Efficient coupling of devices to waveguide wafers
- **Mass Transfer**
  Scales to high device count as data demands continue to rise
- **Minimized device sizes**
  Significant savings of expensive III-V materials



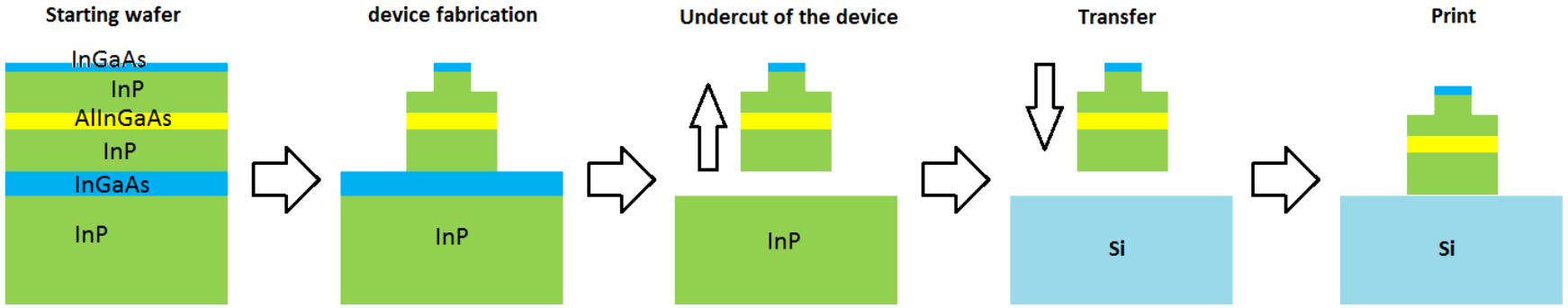




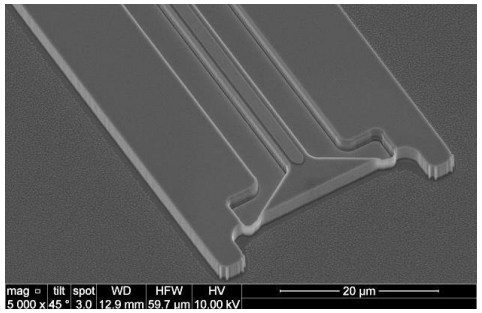


Photonics Lasers

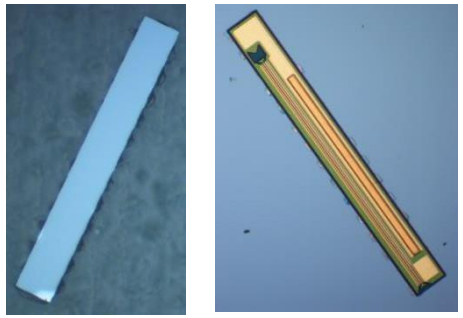
Transfer-Printed InP Lasers



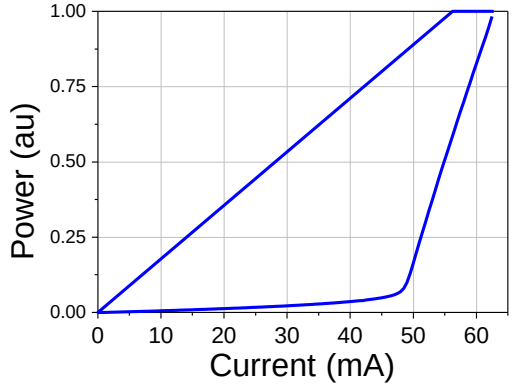
Pre-processed etched facet lasers



Transfer printed to Si



CW lasing of 1550nm laser on Si



Source

Loi, Ruggero, et al. "Transfer Printing of AlGaInAs/InP Etched Facet Lasers to Si Substrates." *IEEE Photonics Journal* 8.6 (2016): 1-10.

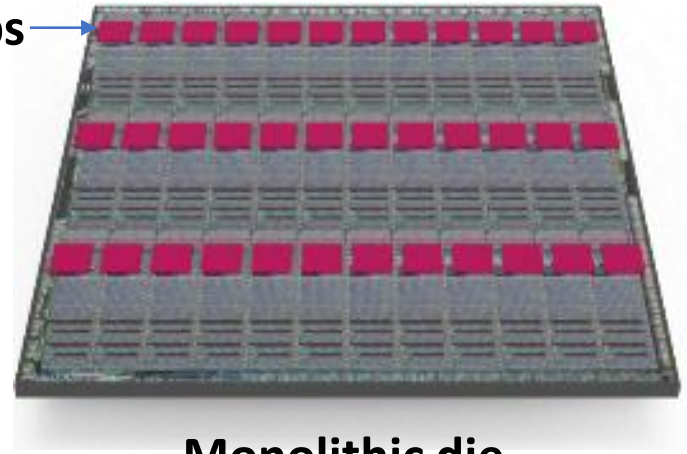
Power 3D IC

Benefits:

- **Disaggregation and tight reintegration of many gate drivers and power transistors**
  - Minimizes parasitics
    Increases switching frequency, density, transient response and efficiency
  - Enables high-performance multi-stage hybrid topologies
- **Cost reduction**
  Produces 3D ICs which resemble conventional 2D ICs (using conventional packaging)

Option #1

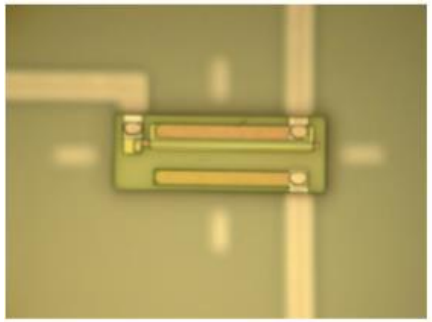
Gate driver x-chips
Loosely-packed SOI



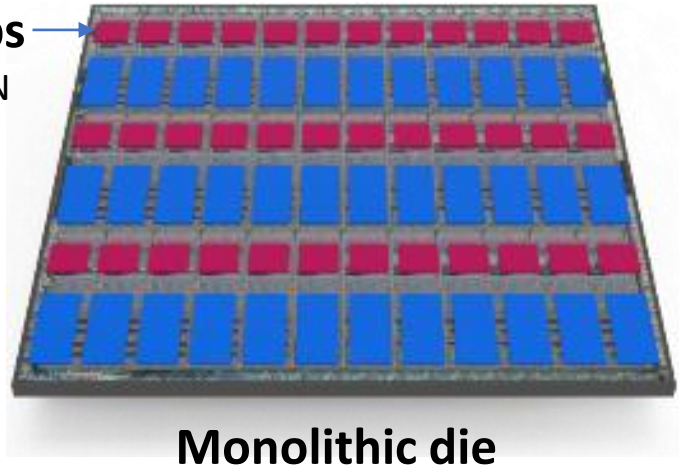
Monolithic die

GaN, GaAs or silicon power transistors
Tightly-packed

Power transistor x-chips
Tightly-packed SOI, GaAs, GaN



Option #2



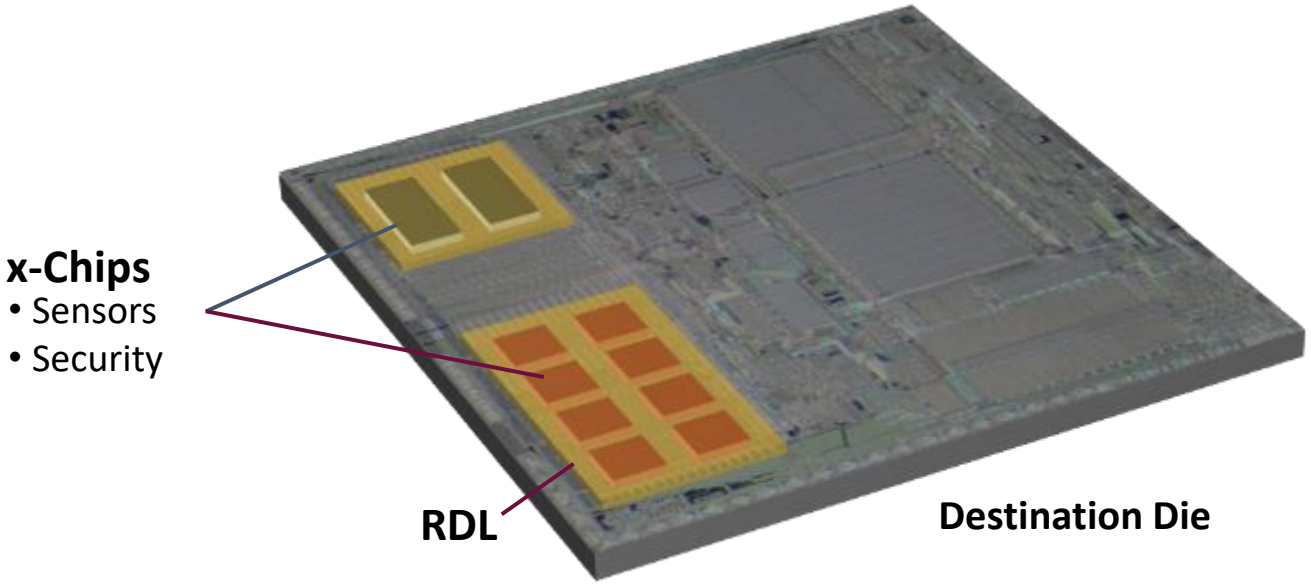
Monolithic die

CMOS IC
Gate drivers, control, protection & monitoring

Secure IC

Benefits:

- **Integrate x-Chips in trusted US advanced packaging facilities**
  Using source wafers produced in US and overseas foundries
- **Provides hardware-based quantifiable assurance**
  For cutting edge ICs produced in untrusted fabs
- **MTP allows for <u>disaggregated</u> arrays of security x-chips**
  Further obfuscate functionality



X-Celeprint's Work-in-Progress

X-Chip

- Large x-Chips over 1mm x 1mm up to 4.5mm x 2.5mm
  - Currently releasing up to 1mm x 1mm square x-Chips and 1.5mm x 100um x-Chips
- Thick chiplets between 50um - 150um thick
  - Currently picking up only released chips proven up to 20um
- Transfer Print from bulk material
  - Standard silicon wafers with no oxide layer
  - III-V material from native substrates
  - Currently using a release layer to undercut chiplets
- Through x-Chip interconnect
  - To allow for additional connectivity through the x-Chip

Alignment

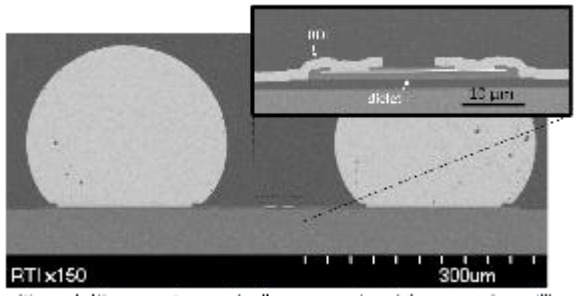
- Roadmap to improve alignment accuracy to 0.5um 3 sigma
  - Currently printing to 1.5um 3 sigma

Summary: Micro-transfer Printing of x-Chips

- **Small devices**
  - At least as small as 3 µm x 3 µm x 200 nm, and likely much smaller
  - As large as 1 mm x 1 mm, and likely larger
- **High throughput**
  - Up to 65,000 devices printed simultaneously in 1 cycle
  - 30 s per cycle
  - ~7M devices printed per hour
- **High yield**
  - >99.9% per print cycle
  - Precision repair → **effective 100% yield**
- **High accuracy**
  - Demonstrated 1.5 µm @ 3σ
  - Working towards 500 nm
- **Small pitch**
  - Down to 2 µm
- **Substrate flexibility**
  - Materials-agnostic
  - Demonstrated print on Si, glass, ceramic, plastic, smooth, & rough surfaces

- **Heterogeneously integrate** different components on one substrate
  - Materials-agnostic
  - E.g., sensors, LEDs, lasers, interconnects, MEMS, etc.
- **Deterministically disperse devices** produced at high density on target surface
- **Vertically stack** chip-on-chip - 3D
  - For 3D HI devices
  - For multi-junction solar cells
- **Simple** thin film interconnect
- End product is highly **customizable and modular**
- **Cost-effective**
  - Efficient use of material
  - High throughput

Key References by X-Celeprint and select partners



Fan-Out Packaging of Microdevices Assembled Using Micro-Transfer Printing

- Interposing of Microelectronics by Micro Transfer Printing to Create 3-D Structures
- Transfer-printing for heterogeneous integration
- Manufacturing Capability of Micro-Transfer Printing
- Scalability and Yield in Elastomer Stamp Micro-Transfer-Printing
- Fan-Out Packaging of Microdevices Assembled Using Micro-Transfer Printing
- Transfer printing by kinetic control of adhesion to an elastomeric stamp
- Kinetically controlled, adhesiveless transfer printing using microstructured stamps
- Process capability and elastomer stamp lifetime in micro transfer printing
- Transferred III-V materials-novel devices and integration